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cover features

IMS2018 Student Design Competion Winners

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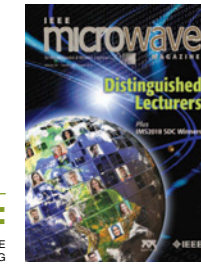

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IMS2018 Student Design Competion Winners (*continued*)

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From the Editor's Desk

2019: More for Our Readers

■ **Robert Caverly**

Even though the issue date says January, as I write this column, summer is turning to fall in the United States (and spring is just starting in the southern hemisphere), which means changes in the weather. However, it is not just the weather that is changing.

Starting with this issue, *IEEE Microwave Magazine* returns to monthly issues: 12 issues for 2019. For you, the reader, this means receiving almost twice as many issues as in 2018, with articles that provide broad overviews of new technologies and historical perspectives on current technologies. For those of you who have written articles and are patiently waiting for them to be published, the wait has grown shorter.

I mention both the reader and the author here because, as the magazine's editor-in-chief, I believe there is a symbiotic relationship between the two that is best summed up by paraphrasing Samuel Johnson (who was actually referring to books, but his remarks are appropriate here as well): "A writer only begins an article. A reader finishes it."

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In This Issue

Professional Features

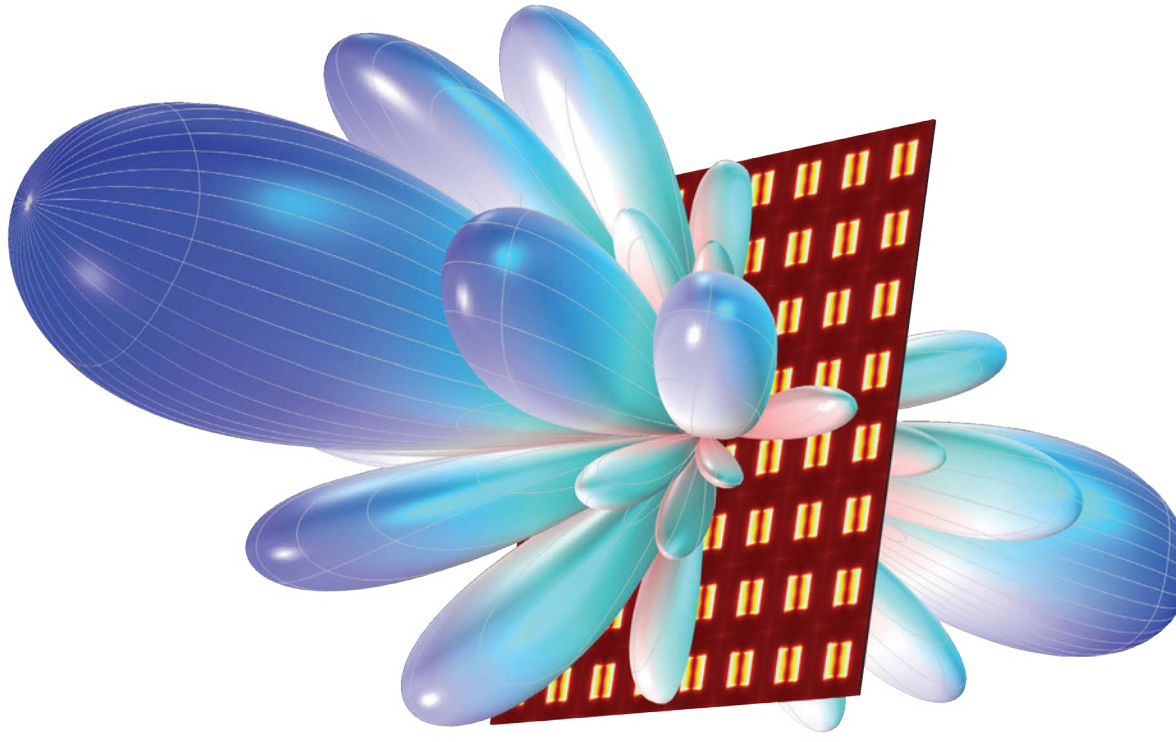
The first two features in this issue of *IEEE Microwave Magazine* are based on presentations by two IEEE Microwave Theory and Techniques Society (MTT-S) Distinguished Microwave Lecturers (DMLs).

- The first, by Dr. Charles Campbell, discusses the evolution of the nonlinear distributed power amplifier. This article contains some interesting design tips for those working in this area, including the need for transformers and how GaN technology has revived this power amplifier topology.
- The second DML article, from a team led by DML Dr. Tian-Wei Huang of National Taiwan University, describes the components of a smart RF integrated circuit (RFIC) for use in a gigabit millimeter-wave transceiver. The authors discuss various subsystems on the chip, with a focus on its self-healing and autoswitching functionality.

The issue's third feature article, from a team led by Prof. Torikul Islam Badal and Prof. Mamun Bin Ibne Reaz, is one that the authors have been patiently waiting to publish. It, too, focuses on RFICs: in this case, for the 2.4-GHz range, using CMOS technology. I thank the authors for their patience while we found space in the editorial calendar for their work.

(continued on page 9)

IoT calls for fast communication between sensors.



Visualization of the normalized 3D far-field pattern of a slot-coupled microstrip patch antenna array.

Developing the 5G mobile network may not be the only step to a fully functioning Internet of Things, but it is an important one — and it comes with substantial performance requirements. Simulation ensures optimized designs of 5G-compatible technology, like this phased array antenna.

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President's Column

Looking to 2019

■ **Dominique Schreurs**

Welcome to 2019, a year during which we aim to increase the IEEE Microwave Theory and Techniques Society (MTT-S) member experience, ranging from young professionals to IEEE Life Fellows! Some initiatives to enhance membership value were already advanced at the most recent MTT-S Administrative Committee (AdCom) meeting in October 2018, which was colocated with the 2018 European Microwave Week (EuMW), in Madrid, Spain.

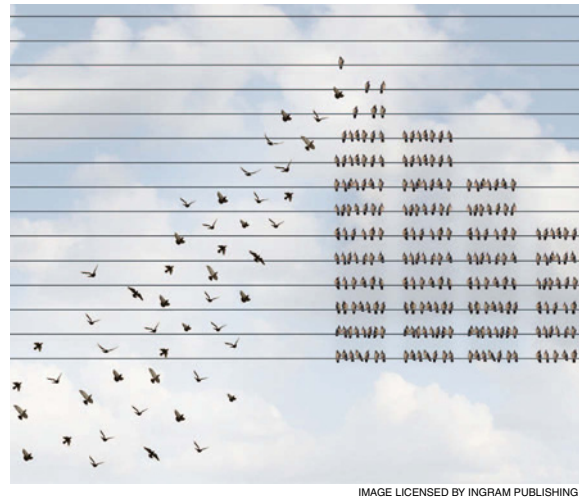

IMAGE LICENSED BY INGRAM PUBLISHING

First, the pilot program to offer reduced conference registration fees to MTT-S members at a select number of MTT-S conferences in the fourth quarter of 2018 will be rolled out on a broader scale in 2019. Due to organizational reasons, the initiative applies only to conferences that are 100% financially sponsored by the MTT-S.

Second, we introduced differential publication page charges for the two MTT-S transactions: *IEEE Transactions on Microwave Theory and Techniques* and *IEEE Transactions on Terahertz Science and Technology*. From 2019 onward, the mandatory overlength page charge will be reduced for authors who are MTT-S members, as compared to nonmembers.

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Other ideas are in the pipeline. Figure 1 shows a brainstorming session among Chapter chairs who were gathered at the September 2018 AdCom meeting. The aim was to exchange best practices and conceive new plans to better serve local MTT-S members. Such Chapter chair meetings are well attended, as Figure 2 suggests. Although the meeting took place in Europe during EuMW 2018, Chapter representatives congregated from around the globe: South Africa, Latin America, the United States, Russia, China, Japan, Australia, and others, all collaborating with multiple European Chapter chairs.

At the close of 2018, several elected AdCom members ended their terms. I would like to recognize the dedication to the MTT-S demonstrated by outgoing AdCom members Dr. George Ponchak, Prof. Shiban Koul, and Prof. Michael Steer for well over a decade. We hope to continue relying on their combined expertise and advice in the years to come.

Finally, I am happy to introduce the 2019 president-elect, Dr. Alaa

Figure 1. *Brainstorming among Chapter chairs at the September 2018 AdCom meeting. (Photo courtesy of K. Ghorbani.)*

Figure 3. *MTT-S President-Elect Dr. Alaa Abunjaileh for 2019. (Photo courtesy of D. Schreurs.)*

Figure 2. *Attendees at the Chapter chairs meeting held in September 2018. (Photo courtesy of K. Ghorbani.)*

Abunjaileh (Figure 3), who is from the United Kingdom and works in industry. He has performed various roles on the MTT-S AdCom throughout the past eight years, most recently serving as MTT-S treasurer.

I hope you enjoy this issue of *IEEE Microwave Magazine*. Note that, as another means of enhancing MTT-S member experience, the magazine has returned to 12 monthly issues for 2019.

From the Editor's Desk *(continued from page 6)*

Student Features

The January issue has traditionally included articles by the winners of the IEEE MTT-S International Microwave Symposium (IMS) Student Design Competition (SDC). In this issue, we continue the tradition with seven articles growing out of the IMS2018 SDCs held in Philadelphia, Pennsylvania. These articles cover a range of microwave technology from wireless power charging to high-efficiency, low-frequency power amplifiers and adaptive compact filters. The articles are written by students and, in some cases, coauthored by their advisors.

These authors represent the future leaders in microwave technology and the future full members and leaders of the MTT-S. Some student articles did not make this issue, but we will make space in future issues for these articles, which will be labeled as SDC winners as well. I encourage you to read both the student and professional articles to "finish" the authors' work.

Concluding Words

Finally, and on a somber note, the MTT-S recently lost two active members: Dr. John Douglas Adam and Dr. George Pierre "Pete" Rodrigue. This issue's "In Memoriam" column honors both with surveys of their individual careers and MTT-S activities to outline the contributions made by each. I appreciate the Memorial Committee's efforts in putting this material together.

MicroBusiness

Canary in the Gold Mine?

■ **Fred Schindler**

Our technologies, the ones RF and microwave engineers and researchers have been working on for decades, are having unprecedented commercial success. Companies are doing billions of dollars of business selling components, subsystems, systems, services, and tools. Our technologies touch virtually every person on the planet. We've enabled worldwide connectivity, location services, information acquisition, security, health care, and entertainment. Our technologies have never been more relevant or valuable than they are now, and there are prospects for even more success with advanced semiconductors, greater use of millimeter-wave and terahertz frequencies, advances in materials, and new concepts in design and integration.

How did we get here? Decades ago, when I first became involved in microwave engineering, we were already successful. Thanks to fundamental research in the early to mid-1900s, microwaves had found applications in communications, defense, and even household kitchens. I worked on microwave semiconductors from the beginning of my career in industry. By then, the research and development of microwave semiconductors had already been underway for many years, but commercial applications were limited. I did most of my work with gallium arsenide (GaAs). The running joke was that "GaAs is the technology for the future, it always has been, and it always will be." Now, billions of people carry GaAs in their pockets every day.

During those times, I was employed in the research division of a large defense contractor. For a several years, I worked under a general manager, a brilliant researcher who had made many important contributions to semiconductor

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technology. In fact, he received the IEEE Microwave Theory and Techniques Society (MTT-S) Pioneer Award. He encouraged us to publish all our research; if we were competent, he insisted, we should have substantially advanced our own work by the time our competitors saw its publication. Competitors would therefore be perpetually trying to catch up. The rest of the company didn't always agree with his perspective, but, fortunately for us, most of the time we needed only his approval to publish.

Our competitors published much of their work, too. This was part of the competition—our articles highlighted the progress we were making and helped us promote our work to those funding our research. In addition, our competition was symbiotic: we were spurred not only to outdo each other; we also learned from each other. Each group made progress, and, as everyone made progress, the technology advanced.

That led to today's success: our technologies are being exploited in myriad ways and are key to tremendous commercial success. At the same time, look at what is being published now. Look at MTT-S's conferences and journals. There are still contributions from industry, but far from the level of decades ago. Today, most articles in our conferences and journals are academic.

With commercial success has come a culture of secrecy. Consider the mobile phone. The major handset manufacturers enforce secrecy as they develop models with the latest new features and capabilities. Nothing is known until the annual grand reveal. We see reports about information leaking in advance and hear about the subsequent jeopardy the person or company careless enough to let the information out can be subject to. It's a very competitive environment.

But it's different than the competition of years ago. Then, it was a competition of ideas and technological advancements. Today's competition is based on the marketplace. There are still underlying technological advancements, but they are subservient. They aren't disclosed, even after the fact. This fuels competitive analysis—where technology companies gain access to competitors' products after they are in the marketplace and then carefully evaluate them to understand how they work. There are even companies that provide competitive analysis services. Eventually, we figure out most of what's new in our competitors' products, but we don't learn about things that didn't work well or technical dead ends.

Recently, I worked for a semiconductor company with significant business in the mobile phone market. The secrecy of the mobile handset manufacturers percolated down to us, and I encountered a very different perspective from what

(continued on page 112)

Microwave Surfing

Knock Three Times . . .

■ **Rajeev Bansal**

We live in frazzled times. Government officials wonder aloud [1] whether our microwave ovens are spying on us, reports of Internet-based scams are rife, and hackers seem to be lurking in every nook and cranny. No wonder that when both government and private organizations worry about data security, they use air-gapped (i.e., disconnected from the Internet) computers for storing and processing their most sensitive information. But is that really good enough? Not if you ask Dr. Mordechai Guri.

IMAGE LICENSED BY INGRAM PUBLISHING

Guri directs the Cybersecurity Research Center [2] at Israel's Ben-Gurion University. The center is dedicated to identifying and exploiting vulnerabilities in electronic systems. For example, one effort [3] demonstrated how to steal data from Wi-Fi routers. More recently, his group turned its attention to breaching fully offline computers [4]. How do they do it? The trick is to coerce the disconnected computer into leaking the desired data through acoustic, optical, or magnetic channels.

How does one force an isolated computer to do one's bidding? Even air-gapped computers need periodic software updates or may be temporarily connected to a removable flash drive. If this seems like a big assumption, keep in mind that malware was successfully introduced some years ago into air-gapped computers in Iranian nuclear labs (the Stuxnet worm) and into Pentagon computers (the Agent.BTZ worm) [4].

Once a Trojan horse has been introduced into an isolated computer, the next step is to alter some behavior of the computer in a programmed fashion that can be detected remotely. For example, in 2016, the team used an acoustic attack "showing that they could use the noise generated by a hard drive's spinning or a computer's internal fan to send 15–20 b/min to a nearby smartphone" [4]. As a video posted with [4] shows, this acoustic channel functioned even when music was playing nearby.

Last year, Dr. Guri's team demonstrated successful exfiltration (pulling data out) from a disconnected computer by modulating its light-emitting diodes in Morse code fashion and picking up the data with a drone outside the facility's window. The optical channel was relatively wide-band, sending a megabyte of data in half an hour [4].

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An earlier version of this column appeared originally in the June 2018 issue of *IEEE Antennas and Propagation Magazine.*

The latest exploit to emerge from Guri's lab is labeled *MAGNETO*. As described in [4],

> By carefully coordinating operations on a computer's processor cores to create certain frequencies of electrical signals, their malware can electrically generate a pattern of magnetic forces powerful enough to carry a small stream of information to nearby devices. The team went so far as to build an Android app they call *ODINI*, named for the escape artist Harry Houdini, to catch those signals using a phone's magnetometer, the magnetic sensor that enables its compass and remains active even when the phone is in airplane mode.

Depending on the proximity of the smartphone, the data could be extracted at up to 1–40 b/s, allowing one to steal a password within a minute [4].

Radio signals generated by computers have been used to spy on their operations (e.g., the now-declassified TEMPEST program used by the National Security Agency). As a result, many secure computers (or computer rooms) are now encased in so-called Faraday cages, making radio-wave exfiltration impractical. However, MAGNETO depends on the variation in magnetic fields for messaging, and it is much more difficult to rein in the covert magnetic communication channel [4]. Time to resurrect NASA's human computer program [5]?

Acknowledgment

I would like to thank my colleague Dr. David Tonn for bringing the story in *Wired* [2] to my attention.

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Health Matters

RadioBio and Other Recent U.S. Bioelectromagnetics Research Programs

■ **James C. Lin**

The U.S. Defense Advanced Research Projects Agency (DARPA) issued a request for proposal (RFP) in spring 2017 by announcing its new research initiative: "RadioBio: What Role Does Electromagnetic Signaling Have in Biological Systems?" [1], [2].

The goal of this project was to "determine if purposeful signaling via electromagnetic waves between biological systems exists, and, if it does, determine what information is being transferred." Although it is not obvious how many proposals were received, there were indications that, by the end of 2017, several classified and unclassified projects had been awarded DARPA grants under the RadioBio program.

The RFP called for clearly identified hypotheses for communication channel(s) with specific predictions and experimental tests that could definitively prove each hypothesis. The goal of RadioBio is innovative and intriguing, especially given DARPA's well-earned reputation for creating breakthrough technologies for national security and beyond. The far-reaching Internet project is an obvious case in point.

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The task of discovering, studying, and comprehending how electromagnetic fields and waves affect the intricate biology of living cellular organisms is not only of fundamental scientific importance but also has practical and technological value. Once the bioelectromagnetic mechanisms for weak cell-to-cell signaling and communication in living organisms have been harnessed, the possibilities and potential applications in data transfer, information delivery, and communication for command and control are enormous.

The challenge of RadioBio is simple and complex at the same time. The challenge is simple because living biological cells have long been known to emit electromagnetic fields and waves, and suitable sensors and instrumentation can detect these signals noninvasively, near the cell or at a close distance.

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Macroscopically, organized cells are capable of generating and emitting detectable electromagnetic signals in the noisy, cluttered environment of living bodies. These signals have been successfully applied to create tools for medical diagnosis and the therapeutic interventions modern medical practice relies on. The abundant examples include electrocardiography and magnetocardiography for the heart, electroencephalography and magnetoencephalography for the brain, electromyography for neuromuscular tissues, and electroretinography for the eye, to name a few. The signals are enabled by the electromagnetic fields and the waves emitted by living cells, tissues, or organs, which are detectable from the human-body surface with specific sensors and electronic instrumentations.

In cardiology, minimally invasive endocardioelectrophysiology of the myocardium is often performed to help assess sources of cardiac arrhythmias inside the heart. Moreover, many biomedical research laboratories regularly use miniature penetrating and patch-clamp microelectrodes to record currents from the efflux and influx of biochemical ions, both intracellularly and extracellularly [3]. However, the spectra of the recordings mentioned are typically low—well below 1 kHz—and definitely not in the RF region above 3 kHz, the band commonly used for wireless communications. These types of low-frequency signals are capable of supporting only very limited information content for wireless communication purposes.

This is not to imply that they are incapable of transmitting meaningful or purposeful messages. In fact, even a low-frequency signal with only 1 b of information may convey a meaningful message in a purposefully designed wireless communication system under specialized circumstances and for special purposes or operational requirements.

The challenge is also complex, and not merely because researchers have yet to report direct measurements of electromagnetic radiation involving kilohertz to terahertz signals from a single cell or cluster of living cells close in or far away. There is a total lack of knowledge about any communication-relevant electromagnetic channel between biological cells or systems or any understanding of what biologically significant information may be transferred intracellularly or extracellularly.

The properties and behaviors of ion channels located at cell membranes are subjects presented in basic textbooks on physiology. Ion channels are critical to regulating the life processes of biological cells and, by extension, in the functioning of higher organs and structures. Some explicit examples include voltage-gated ion channels with their exquisite sensitivity to transmembrane potential difference [4] and mechanically gated ion channels with their unique sensitivity to mechanical cells' deformations, stretches, and movements [5]. Thus, the phenomena of biochemical ionic exchanges through channels at cell membranes, ligands, or neurotransmitters through synaptic junctions in neural cells are well established.

The exchanges of biochemical ions via channels for cell membranes, ligands, or neurotransmitters at synaptic junctions represent movements of electronic charge–carrying ions (or *charge flow*). The flow of electrons forms electric currents, which generate electromagnetic radiation by Ampere's law (a constitutive part of Maxwell's classic theory of electromagnetism) [6]. The emitted and received electromagnetic waves may embed or encode information or signaling for cell-to-cell communication; in addition, they may be involved in intracellular and/or extracellular communication under normal or physiologically stressed conditions. These electromagnetic fields and waves should be amenable to noninvasive detection. Thus, the detected electromagnetic fields and waves would be clearly purposeful; they might also play some essential roles in signaling and communication alongside biochemical ions.

One project could be to design and execute controlled laboratory cell biology experiments using isolated cells and cell clusters in culture, e.g., isolated, identifiable, and viable snail esophageal neurons and neuron pairs. The snail neuronal cell preparations are selected for the enhanced repeatability of results and the ability to maintain cell viability over an extended period of time at room temperature [7], [8]. These experiments may be followed up with other single cells and cell clusters in culture, which potentially may transmit and receive signals via electromagnetic fields and waves.

Of course, it would be important to conduct computational bioelectromagnetic modeling to assess the electronic signaling behaviors of as many intracellular and extracellular components as practicable, with the aim of specifying unique features, signal levels, and bandwidths from ionic current flow and the concomitant electromagnetic radiation. The goal would be to define electromagnetic effects that are purposeful and not just side effects of ionic exchanges.

The working hypothesis could be the characterization of a kilohertz-to-megahertz communication channel derived from acquired data and known facts such as time constants from microelectrode-recorded electrophysiological signals and their fading behavior. A related goal might be developing sensitivity-enhanced passive microsensors, nanoscale biosensors, graphene antennas, and instrumentations exhibiting the proper bandwidth and sensitivity to detect anticipated weak fields in extracellular space noninvasively.

The announcement of the RadioBio program is a big deal for bioelectromagnetics. Among other topics in biology, engineering, and medicine, bioelectromagnetics research explores the effects of electric, magnetic, and electromagnetic fields and waves on living things. The discipline embraces a broad range of topics related to electromagnetic fields and waves over a wide frequency range (i.e., static fields to terahertz) and their interactions with and applications in biological systems such as plants, seeds, mammalian cells, and isolated tissues and organs in animals and humans.

For the better part of a quarter century, the number of cellular devices and variety of uses for wireless electromagnetic fields, including RF and microwaves for security, well-being, medical, and

real-world applications, have grown exponentially in every aspect of modern life. In contrast, funding for bioelectromagnetics research has steadily decreased to a trickle, whether from government or public-sector sources.

The wireless and cellular telecommunications industry has become complacent, and it can easily afford to be, given its institutional and organizational cohorts. Telecommunications companies have nearly free reign to develop and deploy cellular mobile phones and wireless RF devices and services as they see fit, with little regard for the biological effects and health implications of RF/microwave exposure and the considerable amount of unnecessary RF/microwave radiation people are exposed to daily. The U.S. government seems to have all but abandoned the Radiation Control for Health and Safety Act of 1968 and the preceding deliberations that led to its establishment [9].

There is an exception. The U.S. Food and Drug Administration initiated and the National Institutes of Environmental Health Sciences and the National Toxicology Program sponsored and conducted the recently completed US$25 million research on cell-phone RF radiation and cancer in laboratory rodents [10]–[13]. These efforts should be praised and applauded.

Another visible and important role the U.S. government has assumed in recent years, among a handful of bioelectromagnetics research projects, is the U.S. Air Force Office of Scientific Research's Multidisciplinary University Research Initiative grant program. This ongoing program supports fundamental, cutting-edge research that crosses traditional science and engineering boundaries. It focuses on in-depth mechanistic research concerning the interaction between nanosecond-pulsed electric fields and living organisms and the development of targeted stimulation procedures and processes [14].

The importance of the U.S. government's role in sponsoring and conducting such research programs cannot and should not be overlooked in human health and safety research investigations, a vital area of science. The alternative may be to leave the matter entirely to the cell-phone industry (or perhaps, the military–industry complex) with free reign in RF biological effects research—a scary scenario, because we are being continually exposed to more and more varieties of RF and microwave radiation 24 h a day, seven days a week, 52 weeks a year.

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Boston, MA, USA

June 2-4, 2019

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Evolution of the Nonuniform Distributed Power Amplifier

Charles F. Campbell

The emergence of gallium nitride (GaN) monolithic microwave integrated circuit (MMIC) technology has been a real game-changer for high-power amplifier and control components. When compared with the incumbent gallium arsenide (GaAs) MMIC technology, a near order of magnitude increase in output power and power handling was achieved with similar efficiency, noise, and frequency capability. In addition, GaN transistors epitaxially grow on high-thermal conductivity substrates such as silicon or silicon carbide (SiC), helping to mitigate some thermal issues associated with high-output power density.

An early application of this new technology was to increase the output power of existing GaAs-based power amplifiers. These designs were typically reactively matched, with output power in the 1–5 W range. It seemed reasonable at the time to simply substitute GaN device models with the GaAs-based design simulation files and reoptimize. Unfortunately, it was quickly discovered that the high-voltage operation of GaN transistors produced a high-Q, output-equivalent source impedance, and Bode-Fano bandwidth limitations degraded the performance of wide-band, reactively matched designs. For narrow to moderate bandwidths, reactively matched GaN power amplifier

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MMIC attempts were, however, successful and produced significant increases in the output power level. An alternate wide-band power amplifier topology, the nonuniform distributed power amplifier (NDPA), was developed in the 1980s and 1990s using GaAs-based MMIC technology. This architecture, however, was not widely used due to the relatively low-output power level GaAs-based amplifiers produced. This all changed with the arrival of GaN-based MMIC technology. The combination of high-output power density and the Bode-Fano bandwidth limitations associated with reactive matching prompted liberal use of the nonuniform distributed topology for wide-band GaN power amplifier MMICs. Many issues, however, were encountered with early GaN MMIC implementations of distributed power amplifiers. Problems that needed to be solved turned out to be fertile ground for innovation, creative thinking, and reusing concepts from the past. This article describes the evolution, operating principles, and some history of the NDPA.

Why Distributed Architectures?

So what is the fundamental reason for using a distributed approach? Most pre-GaN power amplifiers were designed with reactive matching techniques. To answer this, one has to first consider the reactive matching approach. For the moment, assume that the output of the transistor can be represented by a Norton-equivalent circuit, i.e., a current source shunted by a source admittance. The source admittance that best models the frequency response of microwave power devices is a parallel *RC* circuit with circuit elements $R_P R_P$, and C_P [1]. As mentioned previously, high-voltage operation of a power transistor results in a high-Q output impedance. There is a fundamental restriction as to how well one can match an impedance over a given bandwidth. To quantify this restriction requires evaluating the Bode-Fano integral that best represents the frequency response of the impedance that is being matched [2]. It can be shown that the Bode-Fano limited bandwidth of a transistor output impedance matching network is a function of and inversely proportional to the power supply voltage [3]. An approximate expression for the maximum bandwidth of a transistor output matching network is given by (1).

$$B_W < \frac{4.343 I_{\mathrm{MAX}}}{RL(dB) C_P \beta (V_D - V_K)}. \tag{1}$$

The power supply voltage is V_D, and V_K and I_{MAX} are the knee voltage and maximum current, both of which can be determined from transistor pulsed current-voltage characteristics. The degree to which the load impedance is matched to the Norton-equivalent

Most pre-GaN power amplifiers were designed with reactive matching techniques.

circuit is characterized by the reflection coefficient in decibels, $RL(dB)$. The fitting parameter β typically varies between 1 and 2 and is a function of amplifier tuning. If the transistor is tuned for maximum efficiency, β will be closer to 2. Therefore, high supply voltage and efficient operation results in lower Bode-Fano limited bandwidth. The real part of the Norton-equivalent circuit R_P, normalized to device size, is related to β by

$$R_P(\Omega \cdot mm) = \frac{\beta (V_D - V_K)}{I_{\mathrm{MAX}}(A/mm)}. \tag{2}$$

Both R_P and C_P can be determined directly from load pull measurements, and β can be extracted from the data.

The Bode-Fano limited bandwidth for a GaN HEMT calculated from efficiency-tuned load-pull data is shown in Figure 1. One would generally want a 20-dB or better match for the output stage of a high-power amplifier. For a 20-dB match, the bandwidth will be 6.5 GHz or less for a 30-V power supply. More bandwidth is possible using a lower-power supply voltage or a compromised match. A theoretical limit using an infinitely complex matching network is realized using (1). Such a matching network is not practical, and, in reality, the achievable bandwidth will be less than what is shown in Figure 1.

The Uniform Distributed Amplifier

Given the Bode-Fano limitations for reactive matching, an alternate approach will be required for very-wide-bandwidth applications. It is clear from (1) that bandwidth increases if C_P can be reduced. The reduction in effective device capacitance is the fundamental idea behind distributed amplification. This concept is not new and was first disclosed by Percival in a 1936 patent. Additional early references for vacuum tube-based distributed amplifier circuits date back to 1948 [4]–[8]. A generalized distributed amplifier circuit topology utilizing field effect transistors (FETs) is shown in Figure 2. The input and output transistor capacitances are effectively reduced by absorbing them into artificial transmission line structures [9]–[11]. These artificial transmission lines are formed with series-inductive traces (Z_d and Z_g) and shunt capacitors. Most, if not all, of the shunt capacitance is

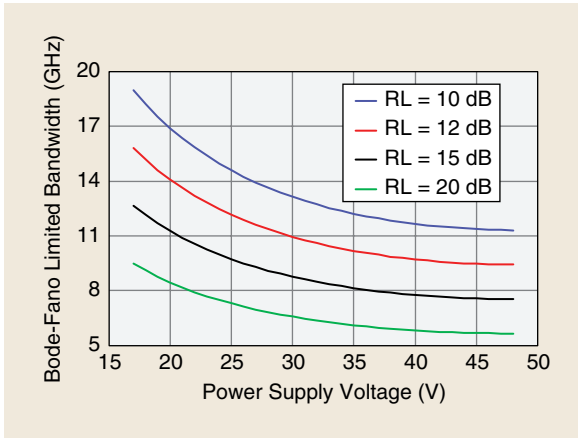

Figure 1. *The Bode-Fano limited bandwidth for an efficiency tuned GaN HEMT at 18 GHz.*

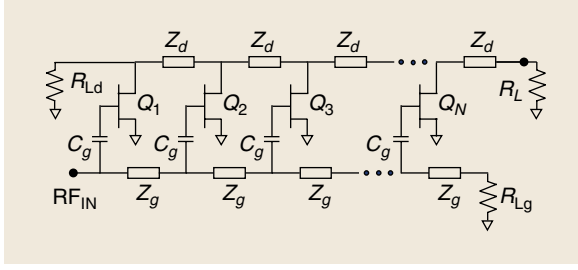

Figure 2. *The uniform distributed amplifier circuit topology.*

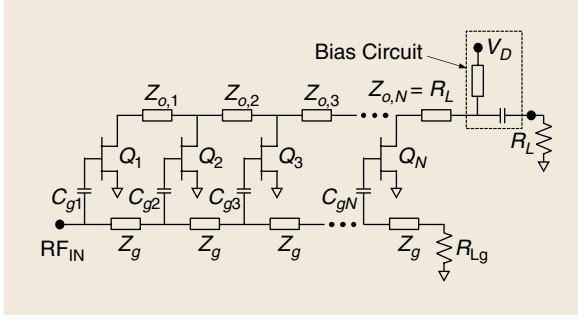

Figure 3. *The NDPA circuit topology.*

supplied by the input and output capacitances of the transistors. This forms a low-pass inductance–capacitance circuit that approximates a transmission line over a finite frequency range depending on how much transistor capacitance needs to be absorbed. The so-called artificial transmission line cutoff frequency reduces as transistor capacitance increases. Because transistor input capacitance is generally higher than that of the output, the cutoff frequency of the input line would set the bandwidth of the amplifier if it were directly connected to the transistors.

To equalize the input and output line cutoff frequencies, additional capacitors C_g are placed in series with the transistor inputs. This series combination reduces the input capacitance seen by the artificial transmission line, thus increasing the cutoff frequency and bandwidth of the amplifier. Some of the input RF voltage will drop across these capacitors, decreasing the circuit's overall gain. In other words, gain is sacrificed for bandwidth, and the gain bandwidth product will remain relatively constant.

As with any transmission line, one of the ports must be properly terminated (R_{Lg} and R_{Ld}) to maintain a good match at the opposite port. The uniform distributed amplifier topology has been used for many years to realize wide-band gain blocks, low-noise amplifiers, and fiber-optic modulator drivers. Unfortunately, this architecture does not function well as a power amplifier. There are a number of reasons for this. First, some of the output signal travels to the left and gets dissipated in the output transmission line termination R_{Ld}. Power dissipated in the output termination is wasted and directly impacts output power and efficiency. Second, the RF input voltage decreases, moving down the input transmission line as each transistor siphons off a portion of the signal. This means that the transistors are not uniformly driven and the devices near the output will contribute less output power than those near the input. The final and perhaps most significant issue is that the uniform distributed amplifier topology does not uniformly or optimally load the transistors. Transistor loading will vary from device to device and over frequency.

The NDPA

To mitigate these issues, the NDPA was developed. A generalized single-stage NDPA circuit topology is shown in Figure 3 [11], [12]. The drain bias circuit is represented as a simple transmission line; however, any circuit that successfully injects the bias into the NDPA without degrading the performance of the amplifier can be used. The NDPA differs from the uniform distributed amplifier architecture in a number of ways.

First, the output termination R_{Ld} has been removed, leaving the output impedance of Q_1 to terminate the line. Second, the input series capacitors $C_{g,n}$ are tapered in size, with smaller-valued capacitors near the input where the signal level is higher. If this is done properly, one can simultaneously equalize the input drive voltage for all the transistors. The tapered input capacitor concept was independently reported in 1984 by Ayasli et al. [13] and Kim and Tserng [14] to improve the output power of GaAs metal–semiconductor FET (MESFET)-based distributed amplifier MMICs.

Finally, the output transmission line characteristic impedances are also tapered in value, with the highest impedance line being connected to the drain of Q_1. The line impedances reduce in value progressing toward the output of the amplifier, with the last line having an impedance equal to the load R_L. By properly tapering the

output lines, each transistor will be uniformly and optimally loaded, at least in theory. An approximate expression for the transmission line impedances can be derived by analyzing the circuit shown in Figure 4 [15], [16].

Here, it is assumed that the device output capacitance has been completely absorbed into the output artificial transmission line and the FET output resistance R_{DS} is large enough to be neglected. The current source in Figure 4 represents the nth transistor in the amplifier. The nth drain node will be loaded with $Z_{o,n}$ looking to the right and have an input impedance of $Z_{o,n-1}$. This node will be driven by the sum of all the transistor output currents to the left of the nth device. The negative sign is due to the transistor current sources being directed out of the connecting nodes. Now, if the nth transistor is to be optimally loaded, the impedance looking into the node where the nth device is connected will be equal to $R_{p,n}$.

Elementary circuit analysis of the network shown in Figure 4 produces the following approximate expression for the output line impedances, where W_{Qi} are the individual transistor peripheries:

$$Z_{o,n} = \frac{R_{p,n} W_{Qn}}{\sum_{i=1}^{n} W_{Qi}} = \frac{R_p(\Omega \cdot mm)}{\sum_{i=1}^{n} W_{Qi}}. \tag{3}$$

One of the characteristic impedances is known, and the last line impedance is $Z_{o,n} = R_L$. Evaluating (3) for the nth transistor results in the following expression:

$$\frac{R_p(\Omega \cdot mm)}{R_L} = \sum_{i=1}^{N} W_{Qi}. \tag{4}$$

Equation (4) is a somewhat unfortunate result and reveals a limitation for the NDPA circuits. For a given power supply and load impedance, the total transistor periphery is fixed for an optimally matched NDPA. The output power capability of the amplifier will be limited by this fixed periphery. To increase output power, one would have to increase R_p by increasing the power supply voltage or somehow decrease the load impedance the amplifier is driving.

Now that the circuit topology and approximate output line impedance values are known, an example NDPA design can be explored. Assume $n = 10$ transistor cells, a 50-Ω load impedance, and 35-V power supply operation. A 35-V supply will result in an R_p around 120 Ω-mm. According to (4), the total device periphery will be 2.4 mm, and one would expect 7–10 W of power from this amplifier assuming 3–5 W/mm of output power density from the transistors. If all transistor cells were the same size, each would have 240 μm of periphery. The output line characteristic impedances as calculated with (3) are plotted in Figure 5(a).

Examination of Figure 5(a) immediately reveals a serious problem. The first few output line impedances are very high. The first line impedance is 500 Ω, which is higher than that of free space (377 Ω). The highest impedance microstrip transmission line that can be realized on a 100-μm-thick SiC substrate is approximately 120 Ω, as represented by the dashed line in Figure 5(a). The first four lines will be unrealizable for a monolithic implementation. No assumptions have been made with regard to the transistor sizes all being the same; they have to sum to 2.4 mm. Making the first device larger and reducing the size of the remaining

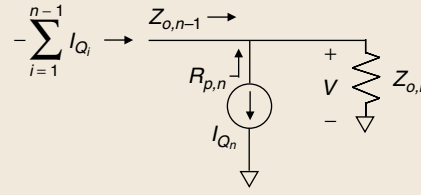

Figure 4. *The simplified equivalent circuit model for the nth transistor.*

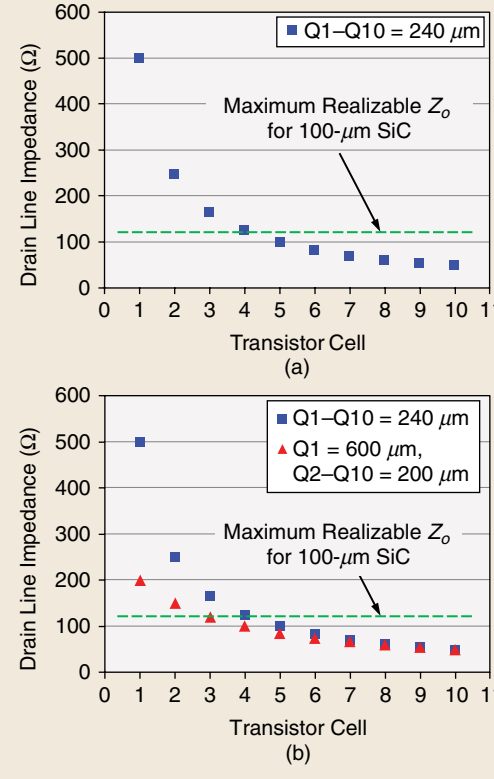

Figure 5. *The output transmission line characteristic impedances for the ten-cell example. The output line characteristic impedances as calculated with (3) for (a) uniform cell size and (b) the size of Q1 increased to 600 μm and the remaining transistors reduced to 200 μm.*

High-voltage operation of a power transistor results in a high-Q output impedance.

transistors improves the high line impedance dilemma to some extent [15].

This is illustrated in Figure 5(b), where the size of Q_1 has been increased to 600 μm and the remaining transistors have been reduced to 200 μm. The situation is better, but the first two lines are still unrealizable. Some practical matters preclude making Q_1 arbitrarily large. High-impedance microstrip lines are very narrow and may not be able to handle the bias current draw from a large device. Larger-periphery transistors also suffer from a reduced level of performance at high frequency.

What If the Load Is Not 50 Ω?

So how does one deal with the problem of unrealizably high drain line characteristic impedances? An alternate expression for the drain line impedances as a function of load impedance can be derived by combining (3) and (4):

$$Z_{o,n} = \frac{R_p R_L}{R_p - R_L \sum_{i=n+1}^{N} W_{Qi}}. \tag{5}$$

According to (5), decreasing the load impedance R_L will also decrease the drain line impedances. Furthermore, a reduced load impedance allows for more device periphery and potentially more output power. Assuming uniform cell size, the calculated drain line impedances for different load values are plotted in Figure 6. For a 12.5-Ω load, all of the transmission lines are realizable for GaN on SiC MMIC processes. Nine of ten lines can be built for a 25-Ω load, and making the first device larger would likely render this case realizable as well.

The drain bias circuit shown in Figure 3 has thus far been neglected from the discussion. High-power amplifiers can draw large amounts of current. The bias circuit must not load the core amplifier over its operational band and reliably support the current draw. The $\lambda/4$ transmission line is a simple bias circuit for which a tractable analysis can be performed. The fractional bandwidth over which a $\lambda/4$ transmission line bias choke presents an impedance that is α times greater than R_L is given by (6), where Z_{choke} is the impedance of the bias line. The value of Z_{choke} is determined by the amplifier's dc draw because the bias line must be wide enough to reliably support this current. Examination of (6) suggests that the bandwidth of the bias circuit increases as load impedance R_L is reduced:

$$\frac{f_H}{f_L} = \frac{\pi - \tan^{-1}(\alpha R_L / Z_{\text{choke}})}{\tan^{-1}(\alpha R_L / Z_{\text{choke}})}. \tag{6}$$

To investigate further, the fractional bandwidth for a few specific cases has been plotted in Figure 7. Here, the fractional bandwidth is evaluated for a bias line capable of handling 25 mA per micrometer of width. The impedance the bias line presents to the rest of the amplifier circuit is at least twice ($\alpha = 2$) that of the amplifier load impedance. It is also assumed that the maximum amplifier current draw is 300 mA per millimeter of transistor periphery used in the output stage. Therefore, given a load impedance R_L and power supply voltage V_D, R_p is determined with (2) and total periphery with (4), from which the amplifier's maximum dc draw and bias line width can be computed. Finally, the characteristic impedance of the bias line Z_{choke} is calculated from the line width, substrate thickness (100 μm), and dielectric constant ($\varepsilon_r = 9.7$).

Fractional bandwidth data are plotted in Figure 7 as a function of amplifier load for different power supply voltages. It is interesting to note that, for this

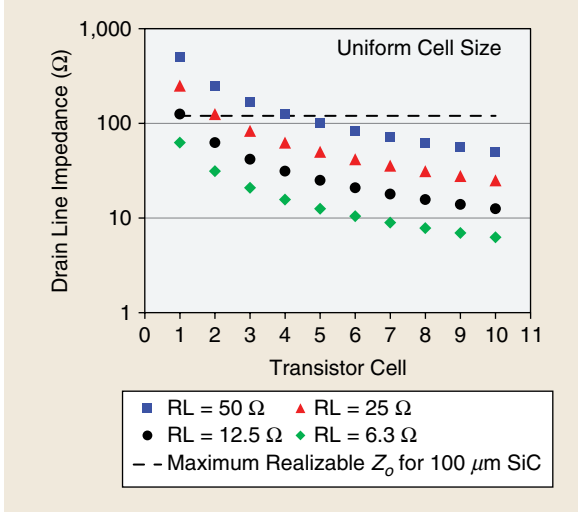

Figure 6. *The output drain line impedances for the ten-cell example with reduced load impedance.*

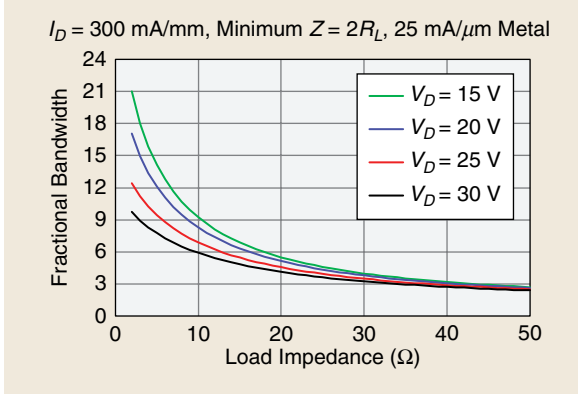

Figure 7. *The fractional bandwidth of a quarter-wave bias line.*

particular case, the industry standard 50-Ω load will result in around 3:1 fractional bandwidth independent of the transistor supply voltage. This will likely be less bandwidth than the cutoff frequency of the gate/drain lines, meaning that the bias line generally sets the bandwidth capability of a 50-Ω loaded NDPA. As the amplifier load impedance is decreased, the power supply has a larger impact, with bias line fractional bandwidth increasing as supply voltage and load impedance are reduced. The analysis strongly suggests that wide fractional bandwidth designs will benefit from a lower than 50-Ω load impedance.

We Are Going to Need Transformers

There is a pretty strong argument developing for using a lower than 50-Ω load for NDPA designs. Most microwave applications require that components operate in a 50-Ω system, and monolithically compatible high-performance impedance transformers will be needed for wide-band NDPA MMICs. Fortunately, such structures do exist.

Monolithic implementations of impedance transformers constructed with lumped elements, stepped-impedance transmission lines, and various connections of coupled lines have all been demonstrated to work well. Two particularly useful examples of the latter are Ruthroff connected coupled coils and, in an MMIC implementation, coupled microstrip lines [17].

The Ruthroff transformer with ideal coupled coils along with an edge-coupled line microstrip implementation is shown in Figure 8 [18]. Assuming ideally coupled coils, the circuit will function as a perfect 4:1 impedance transformer independent of frequency. The microstrip realization does not exhibit perfect coupling and will have a finite bandwidth. Edge-coupled Ruthroff designs on 100-μm-thick SiC have been demonstrated up to 4:1 fractional bandwidth. Another useful feature of the Ruthroff transformer is that the grounded coil is dc coupled to the low-impedance terminal. The ground can be replaced with a bypass capacitor, and the amplifier can be drain-biased through the transformer, mitigating the need for a separate bandwidth-limiting bias circuit. This is the case, provided that the microstrip lines forming the transformer can support the current draw of the amplifier.

Another useful connection of coupled coils is the Trifilar transformer shown in Figure 9 [19]. This circuit can produce a transformation ratio of up 2.25:1, depending on where the low-impedance terminal is connected to the top coil. Although the Trifilar connection has a lower transformation ratio than the Ruthroff transformer, it is capable of more bandwidth. Edge-coupled Trifilar transformer designs on 100-μm-thick SiC have demonstrated up to 10:1 fractional bandwidth. Like the Ruthroff transformer, the ground can be replaced with a bypass capacitor, and drain bias can be injected through the transformer. Examples of NDPA MMICs illustrating the use of these transformer types are presented later in this article.

The so-called artificial transmission line cutoff frequency reduces as transistor capacitance increases.

Early GaAs NDPA MMICs

There are a number of examples of GaN- and GaAs-based NDPA MMICs in the published literature that illustrate the application of these principles. One of the earliest references to what appears to be an NDPA MMIC was reported by Kim and Tserng [14] in 1984. This GaAs MESFET-based MMIC amplifier employs the concept of drive-equalizing input capacitors and tapered impedance output lines [Figure 10(a)]. The amplifier had approximately 5 dB of gain from 2 to 22 GHz. It is claimed in this article that the amplifier produced 0.5 W of output power with an associated 14% power-added efficiency (PAE) at some point in the 2–22 GHz frequency range.

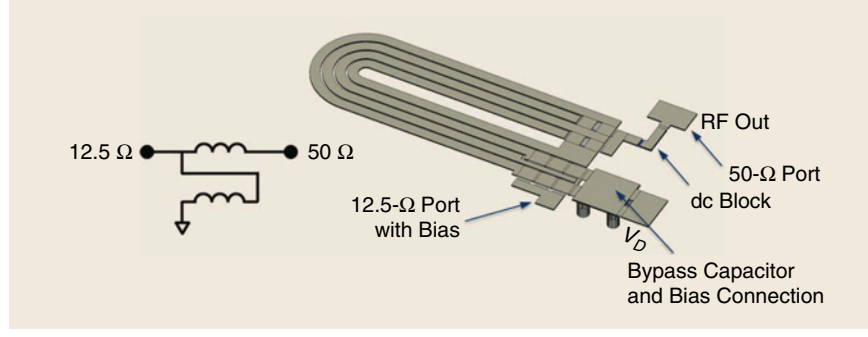

Figure 8. *The ideal 4:1 Ruthroff transformer and an MMIC implementation.*

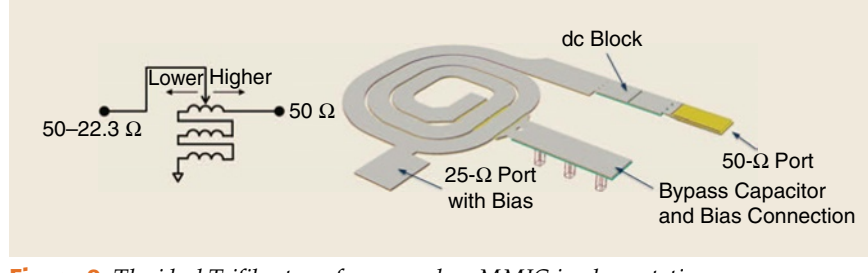

Figure 9. *The ideal Trifilar transformer and an MMIC implementation.*

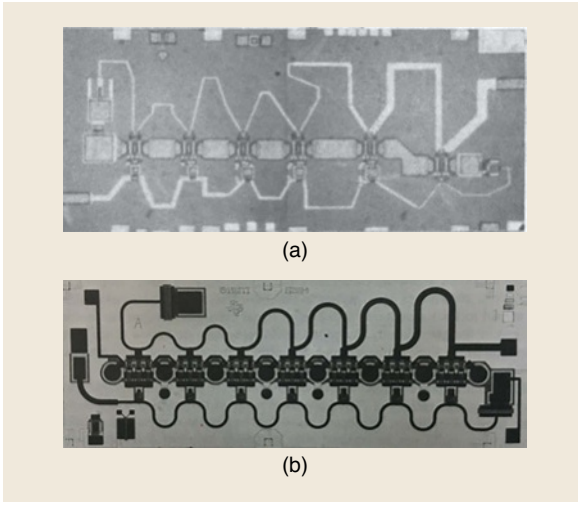

Figure 10. *Early NDPA MMICs using (a) tapered drain lines and (b) tapered input capacitors.*

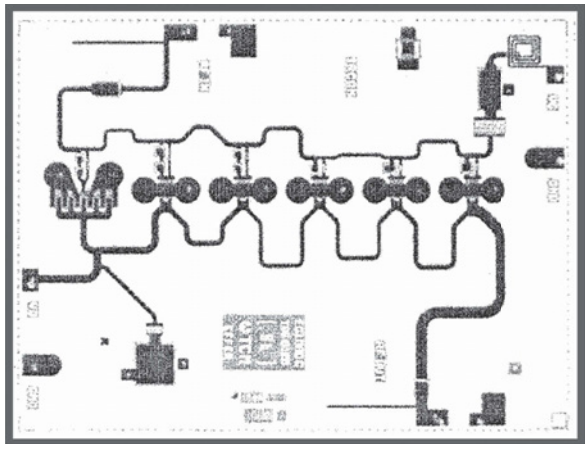

Figure 11. *The NDPA MMIC illustrating the concept of nonuniform transistor size.*

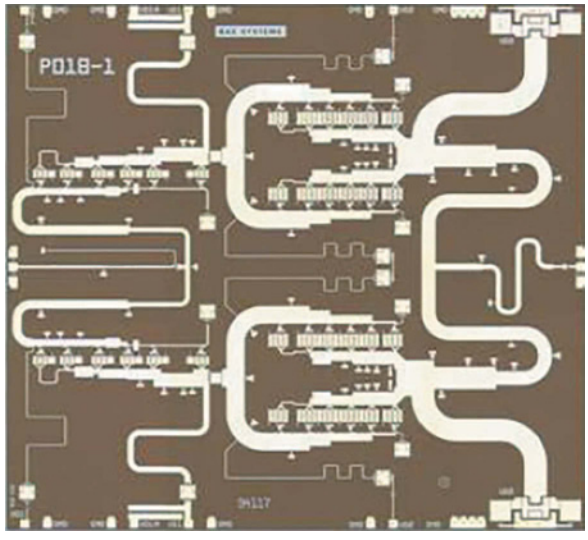

Figure 12. *The NDPA MMIC design utilizing a stepped impedance transformer to reduce load impedance.*

Another early example of a microwave frequency NDPA MMIC [Figure 10(b)] was published by Halladay et al. [20] in 1987. This GaAs-based 0.5-W NDPA MMIC utilized dual-gate FETs and operated from 2 to 18 GHz. The approach of tapered output line impedances and tapered series input capacitors for drive equalization were also used in this design. Drain bias had to be injected with an external bias circuit or a commercially available bias tee for both of these examples.

The GaAs-based design shown in Figure 11 was one of the first to be reported using a larger-periphery first transistor to improve realization of the drain transmission lines [15]. This is apparent in the photograph, where the transistor cell on the left is noticeably larger than the other cells. For some reason, this design did not make use of tapered output line impedances. This MMIC was observed to produce 1 W of output power from 4 to 18 GHz with PAE typically exceeding 20%. The advantages of reducing load impedance were first recognized by researchers developing GaAs pseudomorphic high-electron-mobility transistor-based NDPA MMICs. The lower supply voltage capability and correspondingly lower output power density of GaAs devices necessitated the use of impedance transformation to realize multiwatt-level amplifiers. A stepped transmission line transformer can be clearly seen for the MMIC shown in Figure 12 [21]. This circuit demonstrated 4-W typical output power and 19–31% PAE over a 4–18 GHz frequency range when biased with a 5-V supply voltage. The 50-Ω load impedance is transformed down to 3 Ω, and wide microstrip bias lines successfully cover the operating bandwidth of the amplifier.

Rebirth in the Age of GaN

Though notable work has been done using GaAs-based NDPA MMICs, the low output power density of the available transistors has generally limited the use of this circuit topology. Wide-band, multistage, reactively matched power amplifier designs have proved capable of 3:1 fractional bandwidth with superior output power and efficiency [22]–[24]. It was not until the advent of GaN-based MMIC processes that the NDPA architecture became more widely utilized.

The original pioneering work on GaN MMICs was performed by Lester Eastman's group at Cornell University, Ithaca, New York. What is claimed to be the first GaN NDPA MMIC was published by Green et al. [25] in 2000. This coplanar waveguide circuit operated up to 10 GHz and producing about 2 W of output power at 20% PAE. The design utilized nonuniform output line impedances with the output termination removed.

Higher output power and wider bandwidth results soon followed. The next year, the same research group reported on an MMIC with a range of 5–7 W and dc of 8 GHz that utilized cascode transistor cells [26]. In 2007,

an MMIC with a range of 2–15 GHz and 5–7 W was published by Gassmann et al. [27], and a design including a range of 3–18 GHz and 2 W was reported by Meharry et al. [21]. In a 2011 publication, Pengelly et al. [28] showed results for a dc to 6-GHz NDPA MMIC that utilizes cascode transistor cells such that the power supply voltage can be doubled. This amplifier was, however, dc coupled so that an off-chip drain bias circuit had to be used. The circuit demonstrated 20–30 W of output power and 25–60% PAE under 50-V power supply operation. Most of these benchmarks were established using single-stage amplifiers designed for 50-W load impedances. In 2011, Komiak et al. [29] reported on a two-stage NDPA MMIC that featured impedance transformation and wide-band quadrature combining using Lange couplers. Measured results for this amplifier show 14–27 W of output power over a 1–7-GHz frequency range.

The aggressive design goals of the wide-band track in the U.S. Defense Advanced Research Projects Agency (DARPA) Wide Bandgap Program for RF Applications (WGBS-RF) encouraged further development and optimization of the NDPA architecture. The program specifications called out an amplifier with a range of 2–20 GHz with more than 10 W of output power. The 10-W output power level could not be easily achieved by existing GaN devices that exhibit a high level of performance at 20 GHz. Furthermore, designing a drain bias circuit that could support a 10-W current draw over a bandwidth range of 2–20 GHz was also a challenge. The NDPA MMIC and measured results shown in Figure 13, although not developed under DARPA, did approach the program's performance goals [16]. This amplifier is a ten-cell design and uses many of the performance-enhancing concepts previously discussed. The load impedance is 50-Ω over the lower portion of the operating band, where a higher level of device performance is available. A quarter-wave transmission line transformer is used to reduce the load impedance for the upper part of the operating band and so increase output power near the upper band edge. The bandwidth of the spiral bias choke is increased by its elliptical shape and by suspending it over the substrate using airbridge technology. Experimental results for this amplifier demonstrate 9–15 W of output power and 20–38% PAE over a frequency range of 2–17 GHz. In 2011, a 2–20-GHz bandwidth NDPA MMIC was reported by Komiak et al. [30] based on a two-channel architecture with stepped impedance transmission line transformers that transform down from 100 Ω instead of 50 Ω. This allows the two channels to be directly connected at the 50-Ω input and output ports. The MMIC amplifier shown in Figure 14 produced 10–21 W of output power over the band range of 2–20 GHz.

More complex higher-performing NDPA MMICs followed these benchmarks. Innovations included,

The design and performance of NDPA MMICs has come a long way from the simple, single-stage, externally biased designs of the early 1980s.

multiple-stage designs, the use of higher-speed, short gate-length transistor processes, and wide-band coupled line impedance transformers. An example of a two-stage NDPA that utilizes a Trifilar transformer is shown in Figure 15 [31]. The wide-band transformation capability of the Trifilar circuit resulted in a frequency range coverage of 1–8 GHz for this amplifier. The first output stage

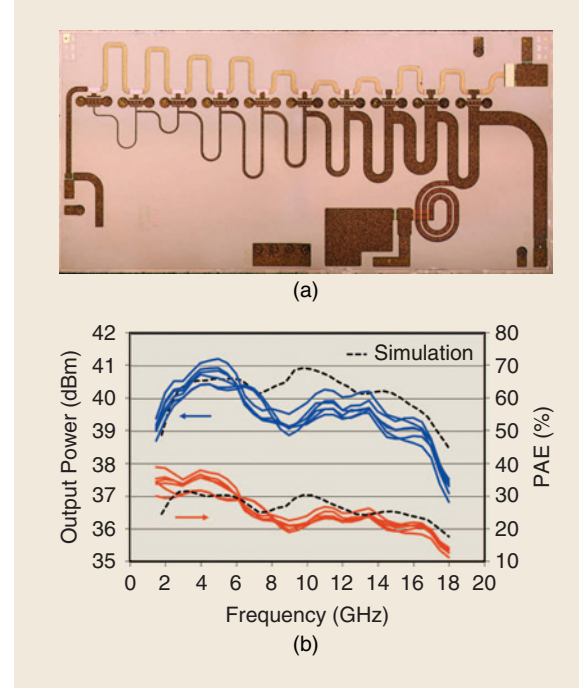

Figure 13. *The (a) GaN-based NDPA MMIC illustrating the use of a quarter-wave transformer to reduce load impedance and (b) the measured results.*

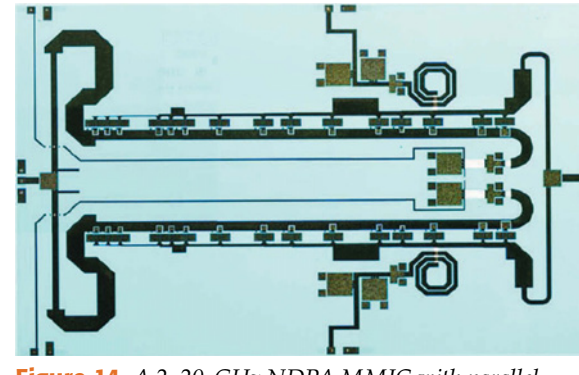

Figure 14. *A 2–20-GHz NDPA MMIC with parallel amplifier channel combining.*

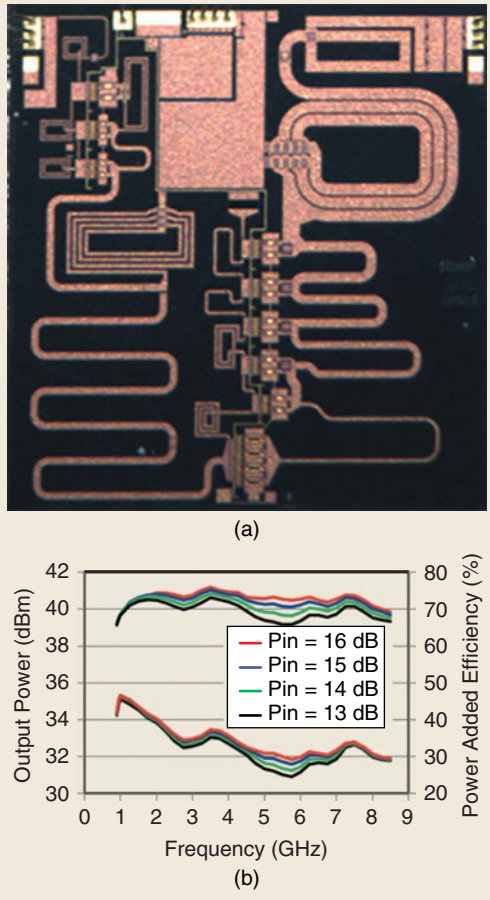

Figure 15. *A two-stage NDPA MMIC illustrating the use of (a) a Trifilar transformer to reduce load impedance and (b) the measured results. Pin: input power.*

transistor has a larger periphery to render the connected drain transmission line realizable. This amplifier is also biased through the transformer structure, eliminating what would be a large bias choke that is nearly impossible to implement monolithically. Recall from Figure 7 that the fractional bandwidth of the quarter-wave bias circuit is around 4:1 for a 25-Ω load. The only practical way to monolithically bias this 8:1 fractional bandwidth NDPA is through the transformer. Experimental results for this MMIC at 16 dBm of drive show 9–12 W of output power and PAE typically exceeding 30%.

Published performance benchmarks for NDPA MMICs eventually pushed into the millimeter-wave frequency range. Dennler et al. [32] presented a two-stage NDPA in 2014 that produced more than 1 W of output power from 6 to 37 GHz. In 2015, Smith et al. [33] reported a two-stage NPDA design that demonstrated 10-16 W of power over a 17–43-GHz frequency band [33]. Another high-frequency example is illustrated in Figure 16 [34]. This three-stage NDPA utilizes Ruthroff connected coupled lines to transform the 50-Ω load to 12.5 Ω and

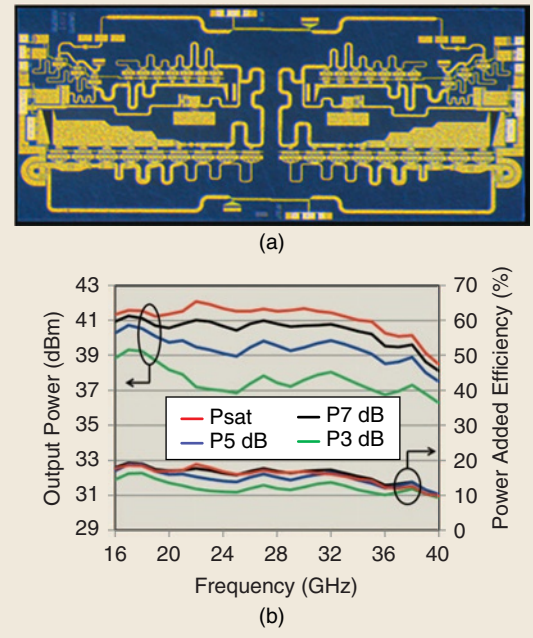

Figure 16. *A three-stage NDPA MMIC illustrating the use of (a) a Ruthroff transformer to reduce load impedance and (b) the measured results. Psat: output power when saturated.*

provide bias to the output stage. Two three-stage channels are then power-combined with Lange couplers to produce 7.5–15.8 W of power from 16 to 40 GHz.

Conclusions and Potential Future Work

The design and performance of NDPA MMICs has come a long way from the simple, single-stage, externally biased designs of the early 1980s. Some of the key developments were the use nonuniform drain line impedances, tapered input capacitors, nonuniform transistor sizing, and load impedance-transforming circuits. For additional benchmarking and historical information for both uniform and nonuniform distributed amplifier MMICs, review the publications by Komiak et al. [7] and Nikandish et al. [8].

As impressive as recent published NDPA MMIC results are, there is still room for improvement. One topic for future work is monolithic transformer improvements. As shown in this article, GaN-based NDPAs generally require a reduced load impedance. Several things may account for this including realizability, wide-band biasing, and increased output power. At low frequency, high-performance transformers are available as off-chip components. Why not have the transformer be external to the MMIC? Unfortunately, at microwave frequency it is very difficult to use an off-chip transformer. Shunt inductors may be easier to implement in a low-impedance system, but the opposite is true for series inductors.

Simulations suggest that the inductance of the bondwires required to connect an off-chip transformer will negate much of the performance advantage. The transformer usually needs to be monolithically integrated with the rest of the NDPA. Even though MMIC-based transformers have demonstrated good performance, they are the bandwidth-limiting component for most NDPA designs. This is especially true if the amplifier is biased through the transformer, as the bandwidth may have to be sacrificed to make the microstrip traces wide enough to reliably support the amplifier's current draw. There is definitely a need for monolithic transformers with broader bandwidth, higher current capability, and higher transformation ratios.

Another significant problem is that the achieved PAE numbers for NDPA MMICs is, in general, far lower than the capability of the constituent transistors. This gap in performance widens as the amplifiers tend toward higher frequency and more bandwidth. Low efficiency means more complex thermal management systems to avoid reduced lifetime and reliability. Clearly, the transistors are not being loaded as optimally or uniformly as the simplified theory might suggest. Something is going on within the NDPA architecture in practice that significantly detunes the output stage devices. Determining the root cause and a solution to the efficiency reduction would greatly improve NDPA performance and usability.

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Smart RF Integrated Circuits

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Increasingly, people around the world embrace the benefits provided by smart phones, smart cars, and smart homes. The key difference between smart phones and traditional mobile phones is the user-defined functionality that enables individuals to transform their phones into music players, movie theaters, or personal workstations. Smart cars with video sensors, lidar sensors, or even millimeter-wave (mm-wave) radar may be autonomously driven. When more and more user-defined

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functions/sensor capabilities are built into RF integrated circuits (RFICs), they are known as *smart RFICs*.

Auto-gain control (AGC), which has traditionally been applied to RFICs, is useful for its amplitude-sensing capabilities. When frequency and phase sensing are present in RFICs, the circuits employ automatic band switching and phase adjustment.

Typically, amplitude modulation (AM) radio and frequency modulation (FM) radio use AM and FM/phase modulation (PM), respectively. To implement a quadrature AM (QAM) digital radio, both AM and FM/PM techniques are necessary for achieving adaptable constellations with process, voltage, and temperature (PVT) variations.

Frequency Sensing: Autoband-Switching Ultra-Broadband RFIC

The function of a frequency sensor is to detect whether input is in-band or out-of-band, as shown in Figure 1. A tunable frequency source, used to approximate and isolate the unknown input frequency, normally requires extra dc power consumption and tuning time. Our proposed design uses a coarse band-switching sensor to quickly discern whether an input frequency is in-band or out-of-band. We determined from our research on a Miller divider that it can be used as a band-switching sensor.

Using Miller Dividers as a Frequency Sensor

The injection-locked frequency divider (ILFD) shown in Figure 2(a) is a single-ended input to a cross-coupled complementary–metal-oxide-semiconductor (CMOS) resonator, while a Miller frequency divider is a differential input to a cross-coupled CMOS resonator. The ILFD has a self-oscillating feature that generates a self-oscillating, free-running output when there is no input; a Miller divider, on the other hand, has a nonself-oscillating feature that generates no output when there is no input.

When there is an in-band input, both frequency dividers can generate locked half-frequency, large-output signals under the frequency-locking condition. For both the ILFD and Miller divider, however, when there is an out-of-band input, the ILFD will generate a large multitone waveform because of the unlocked circuit behavior, while the Miller divider will generate a small harmonic output.

Therefore, when using the Miller frequency divider, we can design a sensor to distinguish whether the signal is in-band or out-of-band. When the input signal is in-band, there will be a large amplitude output; when the signal is out-of-band, there will only be a small harmonic output. A frequency sensor can then be designed with an amplitude detector and cascaded with a Miller divider, as seen in the photo of the chip in Figure 3.

The frequency-band switches inside the Miller divider are controlled by a finite-state machine with the

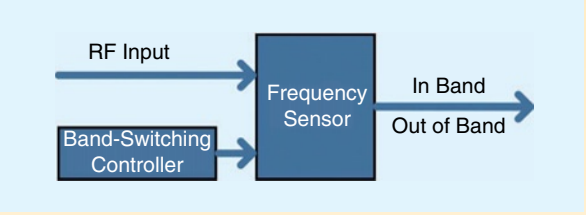

Figure 1. *A band-switching controller can switch to the correct frequency by determining whether the input is in-band or out-of-band when using the Miller frequency divider.*

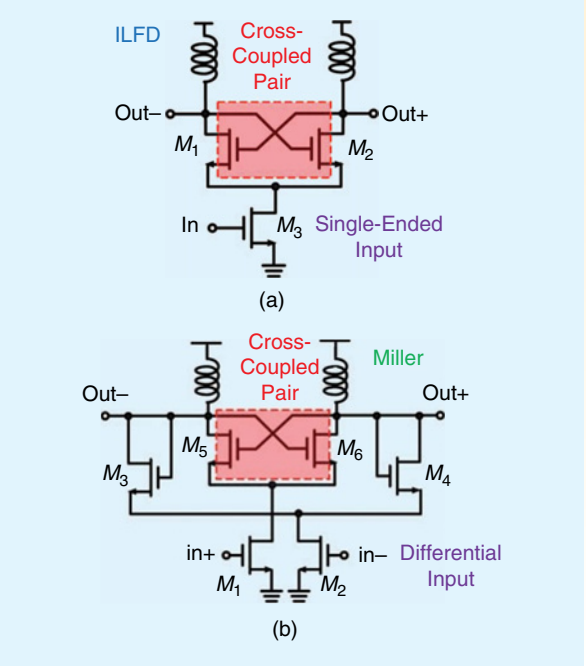

Figure 2. *(a) An ILFD divider and (b) a Miller frequency divider [1].*

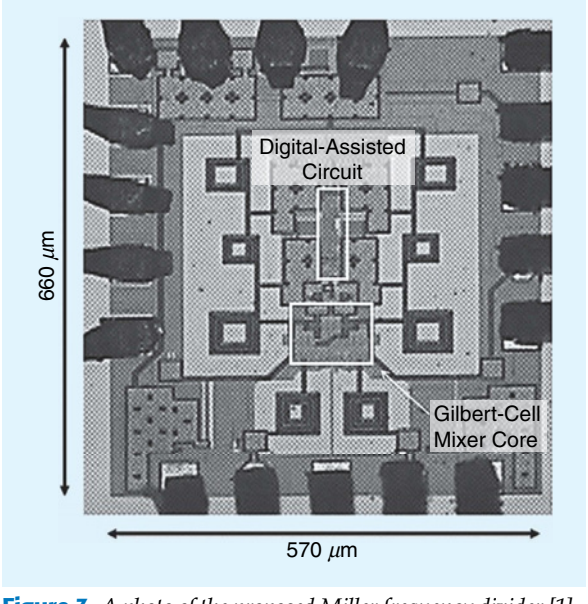

Figure 3. *A photo of the proposed Miller frequency divider [1].*

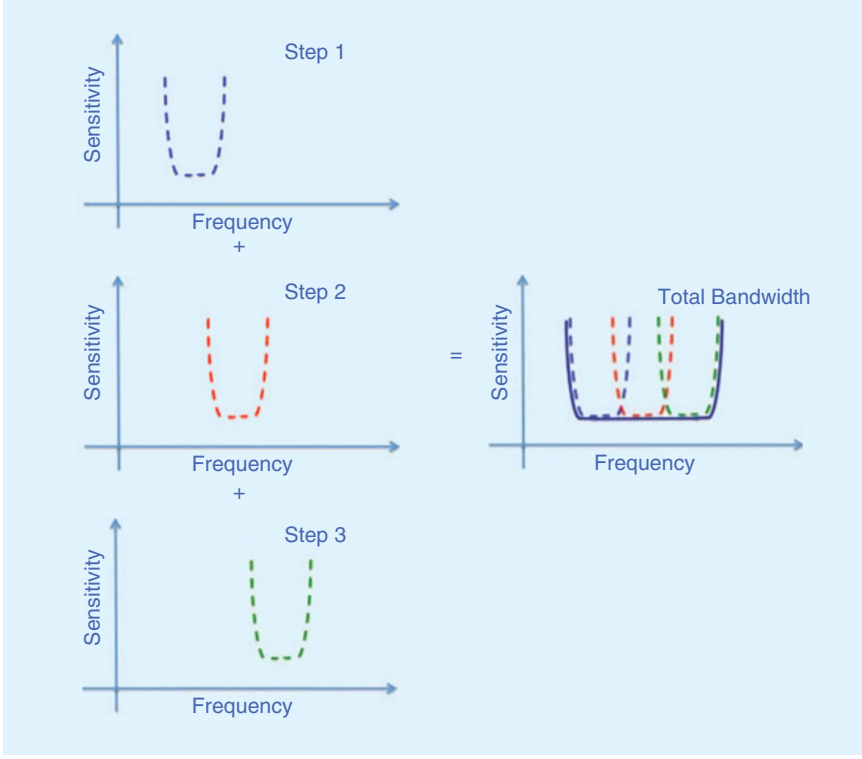

Figure 4. *A frequency sensor that covers the entire bandwidth has a coarse band-switching function to determine whether the input is within any of these three bands.*

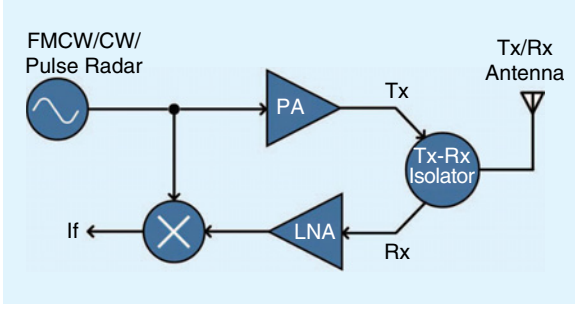

Figure 5. *Single-antenna radar with an on-chip isolator [3]. CW: continuous wave; FMCW: frequency-modulated CW.*

following sequential steps, as shown in Figure 4. We are able not only to detect the input signal within the blue, red, or green bands; we are also able to switch the corresponding operation of the circuit blocks, such as the low-noise amplifier (LNA), mixer, or power amplifier (PA), to the correct band to optimize the circuit's performance. This three-band frequency sensor can complete the detection and switching actions within 40 ns and with below 12 mW. For example, the control signals can be used to change the state of the tunable neutralization transmission lines to adjust the operation frequency of an amplifier [2]. We can then have broadband circuits built upon each band-limited block. The frequency-sensing and controlling techniques can also be applied to the front-end circuits in multiband applications or software-defined radios with fast frequency-hopping capability.

Amplitude Sensing: A Single-Antenna Radar with On-Chip Isolator

For a single-antenna radar transceiver, the transmitter-to-receiver (Tx-to-Rx) leakage signal will degrade the Rx's sensitivity; therefore, the proposed solution (which cancels the leakage signal) employs a passive approach that uses a feedforward technique with a digitally calibrated method, as shown in Figure 5.

The feedforward technique shown in Figure 6 is applied to improve the isolation from 15 to 21 dB by using an out-of-phase auxiliary signal with the same amplitude as the leakage signal to cancel the leakage signal. A digitally calibrated method is implemented to eliminate the need for a manual fine-tuning mechanism for attenuators and phase shifters as well as to mitigate the production issues that are caused by PVT variations during the design process when using the analog feedforward technique.

The feedforward circuit mainly focuses on the leakage signal from the Tx to the Rx. To cancel the leakage signal in the circuit, an auxiliary signal is introduced. The amplitude of the auxiliary signal is adjusted using a T-type resistor network, and the isolation between the main and auxiliary paths is achieved using a Wilkinson power combiner. One way to improve the isolation at the Rx port when combining the main and auxiliary signal is to tune the attenuator; therefore, our proposed solution also incorporates a digitally calibrated design for attenuator control.

To fine-tune the attenuator, a signal is injected at the target frequency so that the main and auxiliary paths have the same signal. Power detectors then sense and convert the amplitude of two-path signals to dc voltage. After comparing the voltages, the successive-approximation-register (SAR) circuit records the binary signal. The SAR then performs a binary search of optimal attenuation to find the optimal code word to control the attenuator through a digital-to-analog converter (DAC), as shown in Figure 7.

The proposed integrated circuit design is implemented in a standard mixed signal as well as the RF 0.18-mm CMOS technology. The Tx-to-Rx leakage signal can be canceled by the auxiliary signal using

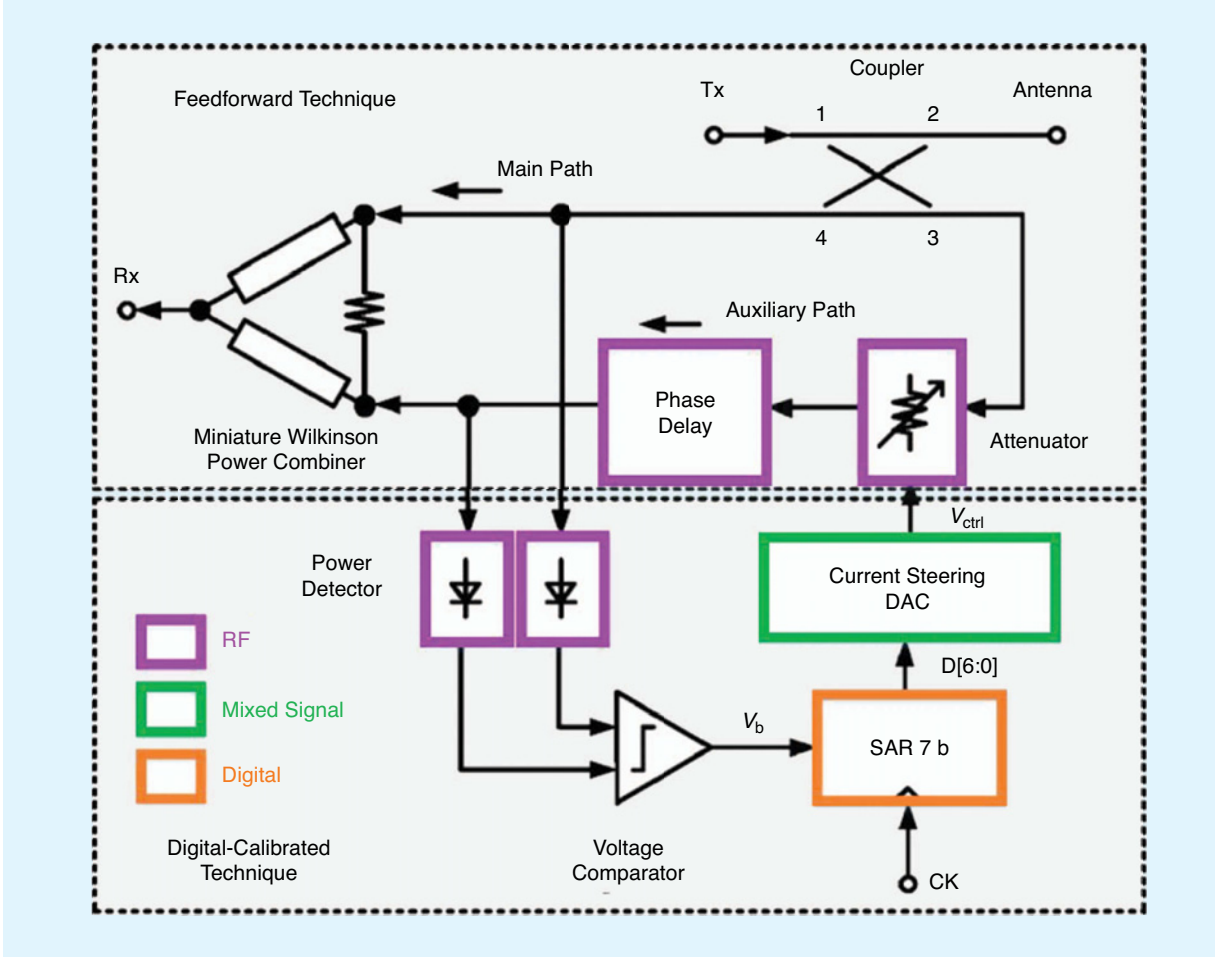

Figure 6. *The block diagram of a digitally calibrated feedforward Tx-to-Rx isolator [3]. CK: clock.*

feedforward circuits with a digitally calibrated technique, which improves the isolation from roughly 18 to 27.3 dB at 25 GHz while using 13.5 mW of dc power. A similar concept of amplitude sensing is adopted in LNAs and PAs. In LNAs, the received signal-strength indicator, error amplifier, and loop filter form the feedback circuit for gain control that allows the LNA to operate in different gain modes [4]. In PAs, the power detector is used to sense the operation power so it can adaptively optimize its efficiency [5]–[6].

Phase Calibration: Digital Phase Shifter

Phase shifters are a critical block in phased-array systems and can also be used as tuning knobs for smart RFICs. Insertion loss, phase and gain errors, phase coverage, power consumption, and chip area are the main considerations in a phase-shifter design. Passive phase shifters are commonly observed and utilized for their low dc power consumption and high linearity [7]–[9]. This passive type of phase shifter usually consists of filters and resonators with digital control. To compensate for high-insertion loss as well as gain and phase variations,

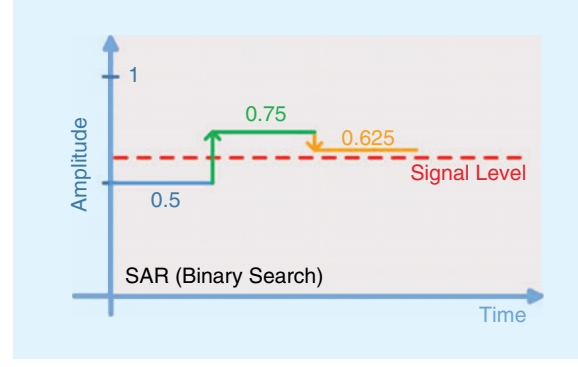

Figure 7. *A digital auto-gain control using an SAR and a DAC.*

a phase-invariant, gain-compensation variable-gain amplifier (VGA) is necessary and can be designed using multiple amplifier stages with opposite phase variation in different phase-shifting modes [10]–[11].

To reduce phase error, phase and gain variation, and phase-tuning complexity in a phased-array system, a 57–64-GHz, low-phase-error 5-b switch-type phase shifter is designed with a low-phase-variation

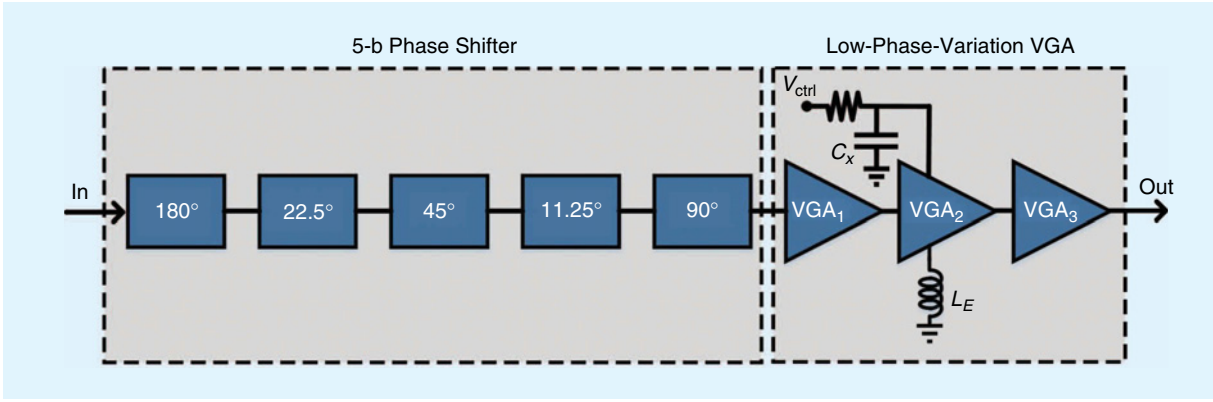

Figure 8. *A block diagram of the proposed 5-b, 60-GHz phase shifter and low-phase-variation VGA [12].*

VGA using 90-nm CMOS low-power technology, as shown in Figures 8 and 9. The developed 5-b phase shifter has only a 2° root-mean-square (rms) phase error while the VGA has only a 1.86° phase variation.

A 5-b Low-Phase-Variation Phase Shifter and Low-Phase-Variation VGA

A previous study [13] demonstrates that a 4-b switch-type phase shifter can achieve a low phase variation of 2°. For our current 5-b phase shifter, we have sequenced the phase-shifting stages by cascading 180°, 22.5°, 45°, 11.25°, and 90°, respectively, to reduce the loading effects from adjacent stages.

After evaluating the advantages of a T-type versus a π-type switch-type phase-shifting stage, the T-type stage, shown in Figure 10, was selected due to its improved phase linearity and group delay. A comparison of the two indicates that the T-type has a much wider bandwidth than the π-type phase shifter for 90° phase shifting, as shown in Figure 11(a) and (b). When comparing the group delays for these two switch-type phase shifters, we can see that the π-type and T-type phase shifters have a group delay deviation of 6.5 and 0.8 ps, respectively, between $V_c = 0\,V$ and $V_c = 1.2\,V$, as shown in Figure 12(a) and (b). Having less group delay for a broadband signal means that there is less phase error; therefore, a T-type phase shifter was implemented because of its superior phase linearity and smaller group delay.

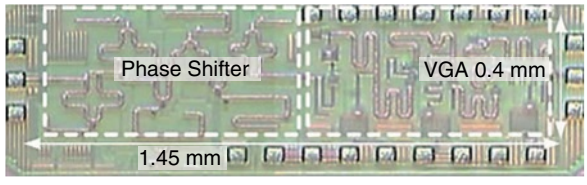

Figure 9. *A chip photo of the 5-b, 60-GHz switch-type phase shifter and VGA [12].*

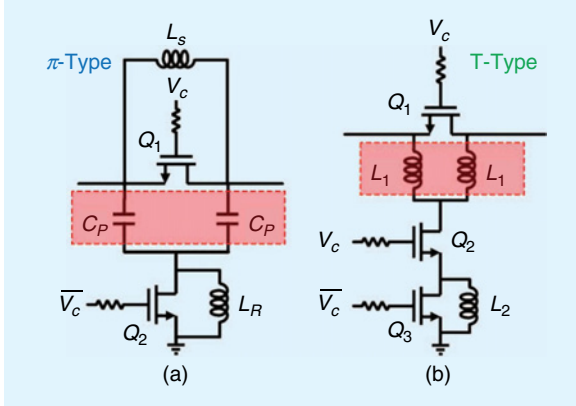

Figure 10. *(a) A π-type switch-type phase shifter and (b) a T-type switch-type phase shifter [12].*

In addition to using a 5-b phase-variation phase shifter, we also implemented a low-phase-variation, three-stage VGA with a phase-compensation capacitor (C_x) and a source-degeneration inductor (L_E) (Figure 8) to significantly reduce the phase variation from 10.5° to 1.5°.

This proposed 57–64-GHz, low-phase-error 5-b switch-type phase shifter with an integrated low-phase-variation VGA using 90-nm CMOS technology reveals a combined rms phase error of 3.3° at 63 GHz. The 5-b phase shifter accounts for 2° of the measured rms phase error at 62 GHz, while the VGA can attain a gain tuning of 6.2 dB with a 1.86° phase variation, as shown in Figure 13. Using a low-phase-variation VGA has a minor impact on the phase variation of the phase shifter, making this suitable for high-resolution phased arrays.

QAM Calibration: MM-Wave 1,024-QAM Broadband In-Phase/Quadrature Tx

When implementing a high-QAM modulator, the most significant issues that impair the RF output are usually related to nonlinearity and in-phase/quadrature (I/Q) mismatch. Achieving higher linearity can be improved by power back-off, but mitigating the I/Q mismatch can only be improved through topology selection and a parasitic-insensitive design methodology. The

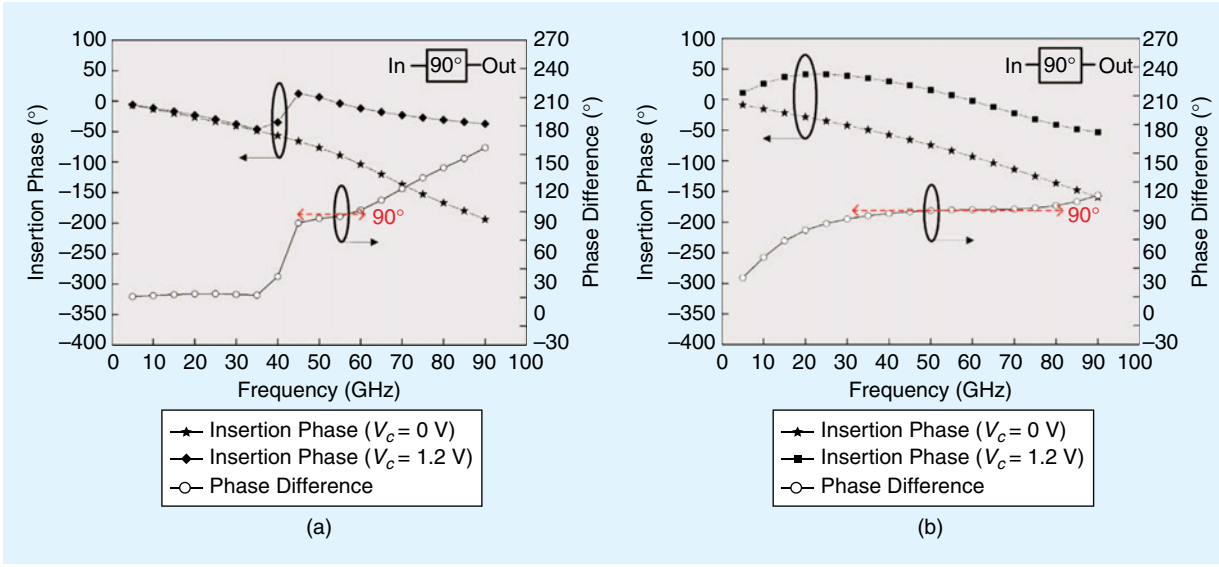

Figure 11. *The phase difference of (a) the π-type phase shifter and (b) the T-type phase shifter in Figure 10 [12].*

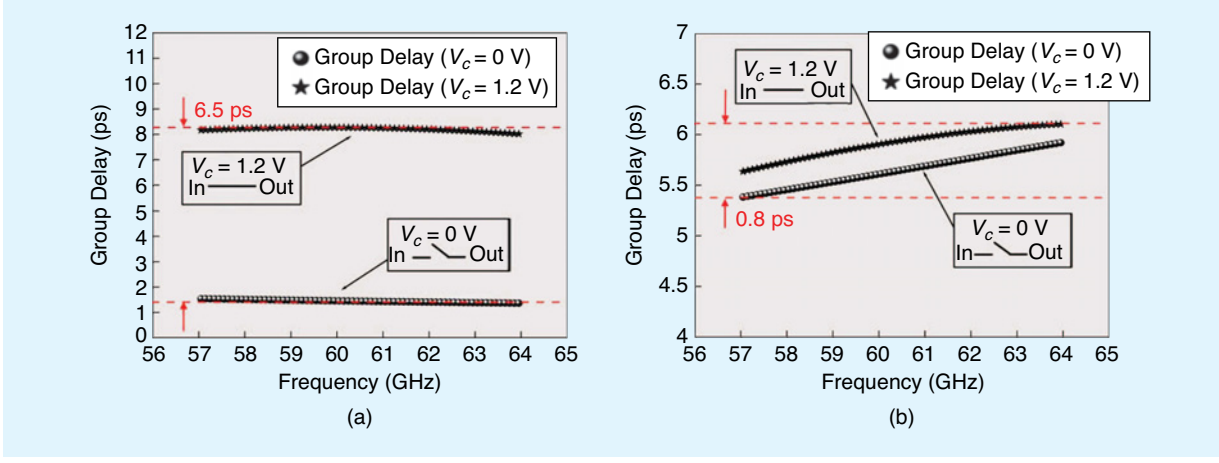

Figure 12. *The group delay of (a) the π-type phase shifter and (b) the T-type phase shifter in Figure 10 [12].*

calibration of I/Q mismatch can be divided into two parts: PM calibration and AM calibration.

The I/Q calibration structure is implemented at the local oscillator (LO) port so that the I/Q balance is less sensitive to the loading effect from the RF port, as shown in Figure 14. The proposed structure can compensate for both amplitude and phase distortion and also achieve a high image-rejection ratio (IRR) for the modulator over a wide bandwidth at high data rates. In the structure shown in Figure 14, a broadband 45° LO power splitter combined with amplitude and phase compensation for subharmonic I/Q modulators can achieve a low-amplitude, phase-imbalanced structure.

For the I/Q mixer to achieve quadrature mixing, an LO signal power splitter with a 45° phase shift is used because the RF frequency is twice the LO frequency in the subharmonic mixer. A 45° phase shift with high-pass filter (HPF) and low-pass filter (LPF) structures provides

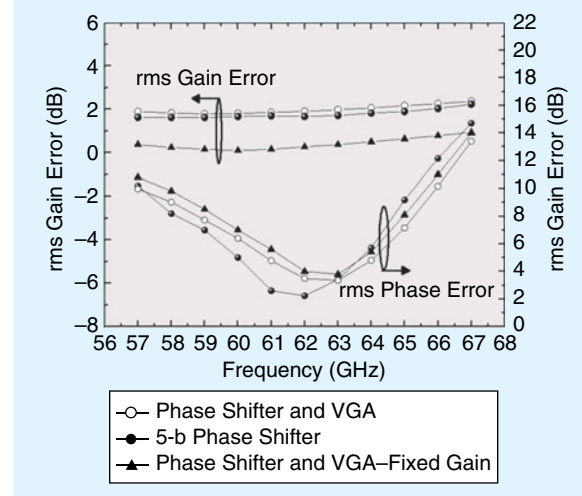

Figure 13. *The rms gain error and rms phase error for a 5-b phase shifter and VGA [12].*

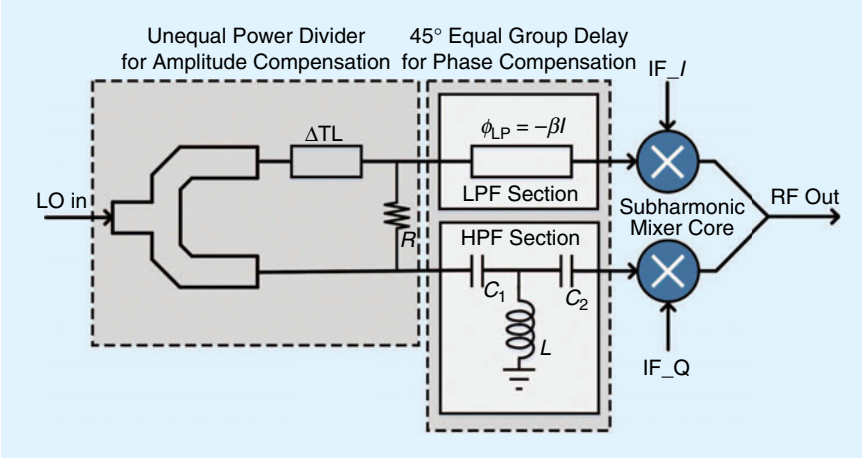

Figure 14. *A 45° phase-shift power splitter with a delay line and HPF/LPF provides amplitude and phase compensation for I/Q calibration at the LO port [14]. HPF: high-pass filter; LPF: low-pass filter. IF: intermediate frequency; TL: transmission line.*

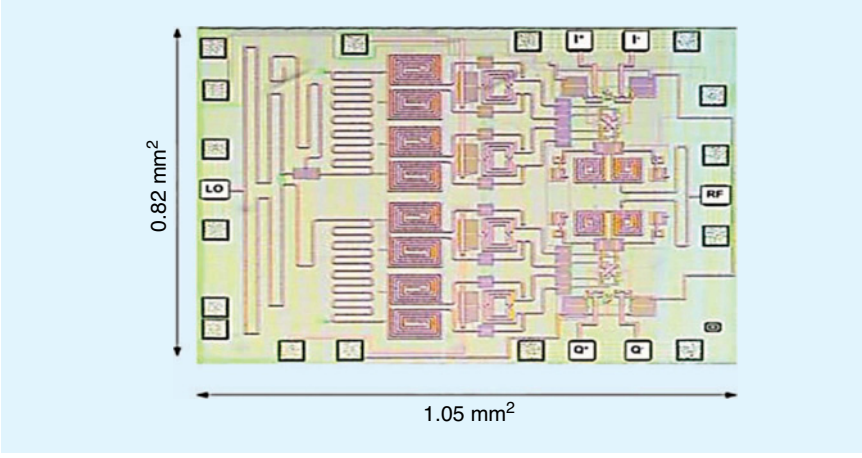

Figure 15. *A die photograph of the E-band modulator [14].*

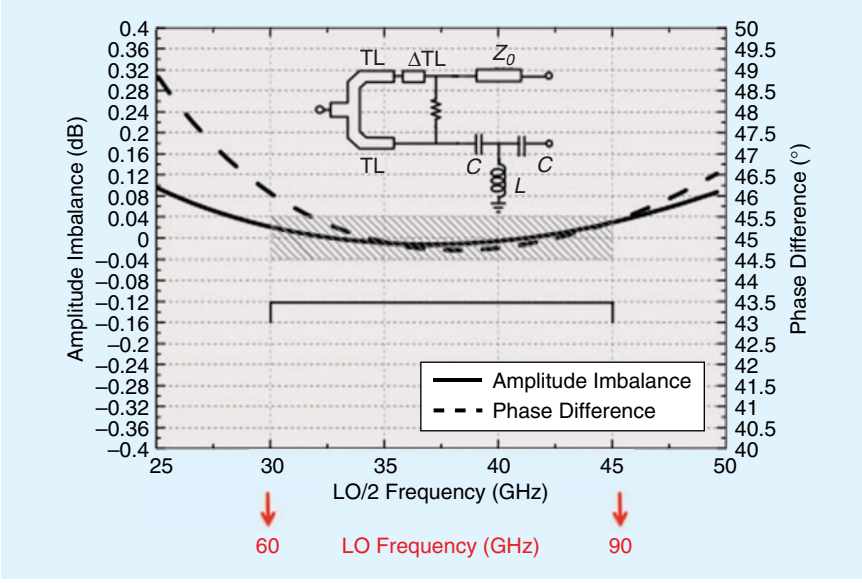

Figure 16. *Combining a delay line with an HPF/LPF helps mitigate both the amplitude imbalance and phase difference [14].*

low insertion loss, broad bandwidth, and a low-imbalance 45° equal group delay. The power splitter also uses an amplitude-compensation circuit to reduce the I/Q mismatch of the entire modulator.

For PM calibration, the combination of an HPF and LPF was selected because the progressive phase of the HPF structure and the phase delay of the LPF structure can create the 45° phase difference between two output ports and result in a broadband, low-imbalance group delay, as shown in Figure 14. When using the HPF and LPF design, amplitude imbalance will occur because the on-chip metal-insulator-metal capacitor, inductor, and transmission lines are not ideal. For AM calibration, a 50-μm delay line (Figure 14) is introduced to compensate for the amplitude imbalance. Due to the phase shift caused by the added transmission line length, the center frequency and phase difference of the LPF and HPF design were adjusted slightly so that both phase and amplitude imbalance can be compensated for at the same time.

For the proposed structure that contains the HPF/LPF and the additional delay line, the amplitude imbalance is <0.04 dB, and the phase difference is <0.5° from 32 to 45 GHz for the LO frequency, as shown in Figure 15. The measured IRR is also greater than 40 dBc for 64–84 GHz, as shown in Figures 16 and 17.

A digitally controlled quadrature error-correction circuit is proposed to lower the error vector magnitude (EVM) of a dual-band Tx [15]. This error-correction circuit consists of four VGAs with different gains, as illustrated in Figure 18. Each amplifier is controlled by 4 digital

bits that adjust the quadrature amplitude and phase mismatches. This correction stage is cascaded with the up-conversion mixer in the Tx. During the error-correction stage, the EVM of the Tx is lowered from 3.21 to 2.8% for a 64 QAM at a 2.4-Ms/s symbol rate and by more than 1% for a 16 QAM at a 3-Ms/s symbol rate.

QAM Calibration: Self-Healing Broadband Transceiver

To further improve the performance of smart RFICs, mismatches and performance degradation due to environmental and process variations in a transceiver can be mitigated using systematic and digitally assisted approaches, such as using a built-in test (BIT) with automatic calibration circuits or by self-healing, which monitors the system performance in real time and employs knob control accordingly [16]–[25]. The accuracy of the sensors, the resolution of the tuning knobs, and the stability and settling of the feedback loop are critical to the healing process. One example of a broadband Rx with BIT is shown in Figure 19. During the self-healing process of the Rx (which consists of an LNA and a mixer), on-chip frequency sources generate RF test signals to the device under test. With feedback performance indicators from the on-chip sensors, the tuning knobs in both the LNA and the mixer circuit blocks can be adjusted to improve the noise figure (NF), linearity, gain, and image rejection.

Specifically, in the Rx, tuning knobs control the dc biases of the LNA and mixer, which are sensitive to PVT. The healing algorithm adjusts the tuning knobs to find the optimal value, as presented in Figure 20. After the signals are downconverted, the biases of the VGAs can be tuned by making differential adjustments to change the gain of the quadrature paths, which improves the IRR from 26.7 to 33 dB, output third-order intercept point (OIP3) from 1.5 to 8.3 dBm, NF from 12.2 to 11.1 dB, and gain from 26.9 to 33.1 dB, with healing.

In addition to tuning the dc bias knobs that optimize the NF, the impedance of the LNA is adjusted digitally to tune the amplifier's frequency response. The entire self-healing LNA includes on-chip sensors, DACs, and digital controllers. With the self-healing technique, the standard deviation of the NF is reduced by 37%, and the 3-dB bandwidth varies between 10.6 and 12.5 GHz with different knob settings [21].

To heal the Tx shown in Figure 21, the probe generator in the self-healing controller (SHC) creates test tones using the numerically controlled oscillators. These test tones can

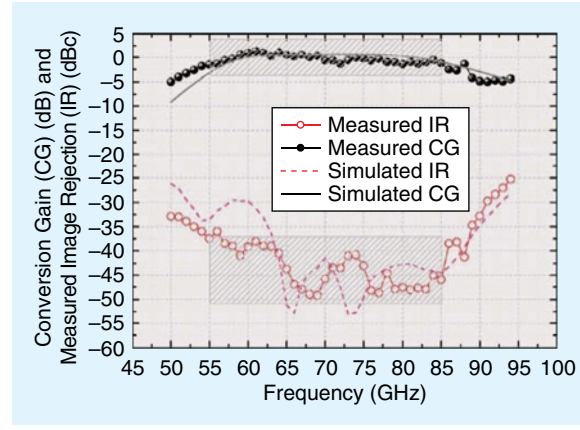

Figure 17. *The measured and simulated conversion gain and image rejection of the E-band modulator [14].*

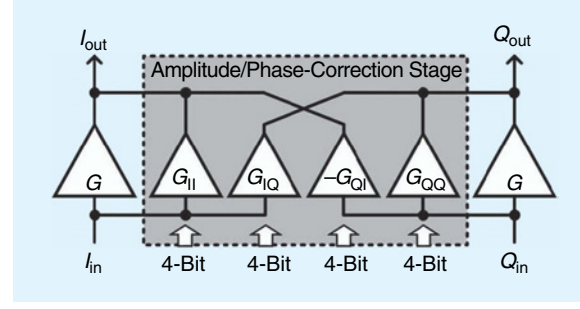

Figure 18. *The amplitude and phase correction using VGAs [15].*

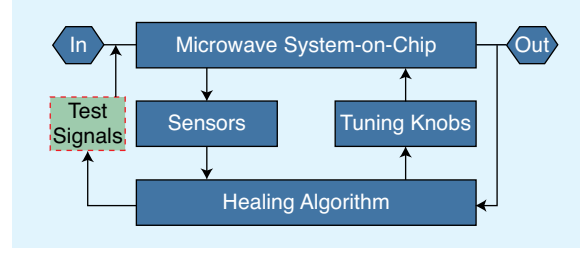

Figure 19. *A block diagram of a general BIT system showing the interconnection between signal sources, sensors, tuning knobs, and healing algorithms [16].*

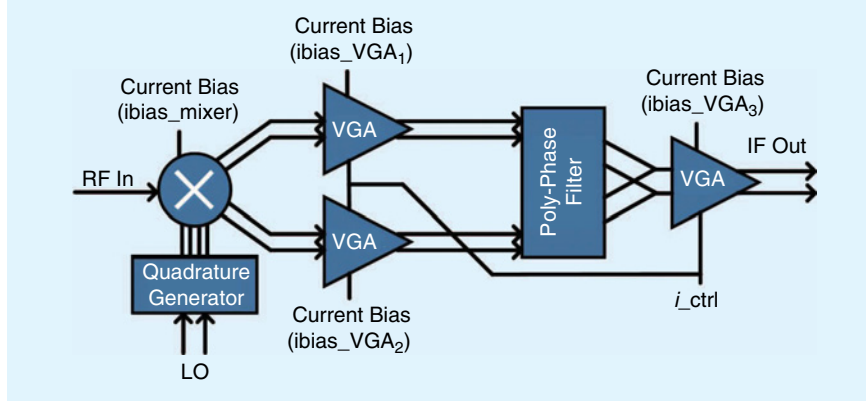

Figure 20. *An 8–18-GHz tunable silicon germanium image reject mixer [6].*

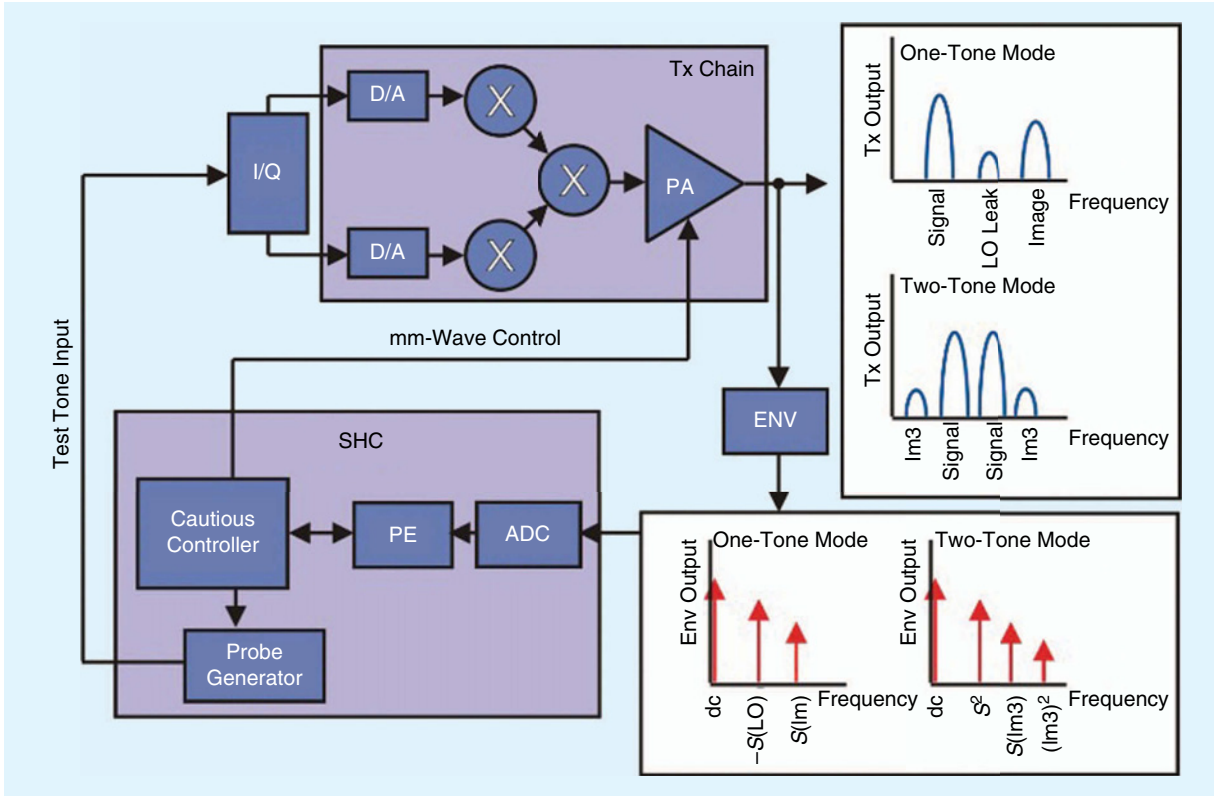

Figure 21. *A Tx self-healing system showing an adjustable Tx chain, I/Q correction unit, envelope (ENV) detector, and SHC [17]. D/A: digital/analog; ENV: envelope.*

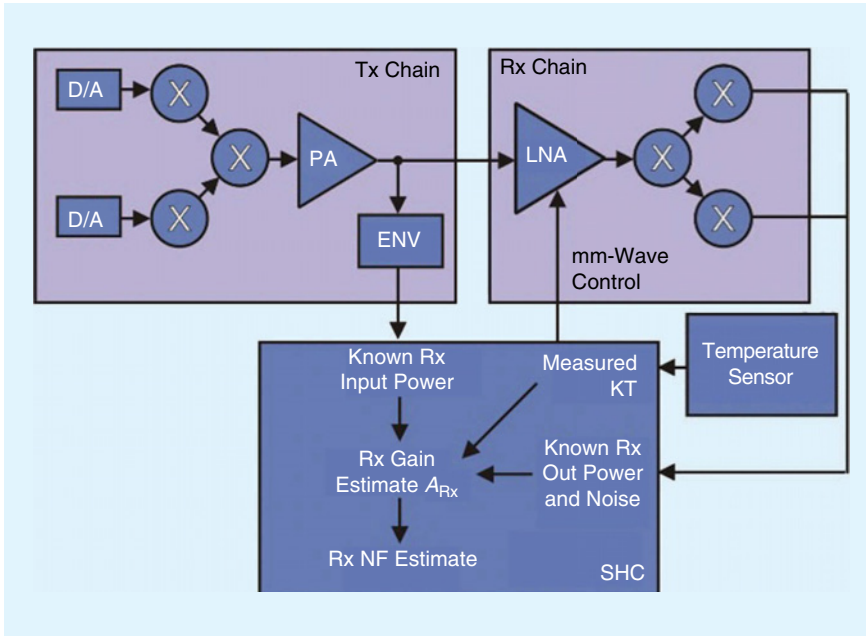

Figure 22. *An Rx self-healing system showing an adjustable Tx chain, adjustable Rx chain, temperature sensor, envelope detector, and SHC [17]. KT: Boltzmann constant times temperature.*

have adjustable frequencies and amplitudes to probe the mm-wave transceiver and measure envelope variations, power levels, and temperature from the transceiver impairments. Based on the performance metrics collected from several different sets of test tones, the coarse searching range and local minimum can be estimated. A thorough search can then be performed around the local minimum to find the optimal spot. The parameter estimator (PE), which contains a 128-point fast Fourier transform (FFT) processor, takes the sensor measurements. The controller can then dynamically change the rate of control for the tuning knobs based on the reliability measures produced by the PE. The 1-dB compression point, third-order output intermodulation (OIP3), and I/Q mismatch can be improved posthealing.

Figure 22 shows the parameters of self-healing in the Rx. Initially, a low-power reference test tone is generated and fed into the Tx to characterize the gain and linearity of the Tx as a calibration phase. Then, the Tx's probe generator creates a two tone. The de-embedded Tx-to-Rx coupling then

computes the power delivered, which is detected using an envelope detector. Subsequently, the SHC's FFT processor detects the tone amplitudes at the Rx output to determine the Rx's chain and then locates the output noise when the Tx is turned off. A temperature sensor subsequently finds the thermal noise floor so that the NF value can be computed to allow bias-current adjustments at each LNA stage.

Using an active self-healing broadband transceiver to calibrate the QAM, gain, NF, IRR, and OIP3 can all be improved posthealing. However, because the IRR reaches only 33 dB, merely using this active QAM calibration with self-healing does not satisfy a 1,024 QAM, we then combine this self-healing technique with the other previously mentioned calibration techniques to achieve a 1,024 QAM.

Conclusions

A smart RFIC requires more user-defined functions and environmental sensors to respond to the changing world. A fast and low-powered frequency sensor is developed using the Miller frequency divider, and a digital DAC can improve amplitude-sensing accuracy. Broadband phase calibration can be implemented through HPFs and LPFs to achieve a broad bandwidth and low-imbalance equal group delay, within a phase error of 1° in the mm-wave frequency. Active QAM calibration through a self-healing technique can significantly improve the transceiver performance, even under PVT variations.

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The fully integrated complementary metal–oxide–semiconductor (CMOS) transmitter (Tx), an essential component in every wireless communication system, ensures highly efficient signal processing and data transmission. The performance of the Tx significantly affects the overall performance of the wireless device [1]. The demand for low-power, low-cost wireless devices operating at the 2.4-GHz band has led to extensive research on RF architecture and circuit design. A well-defined architecture, including linear and simple functional block synthesis, is crucial to the design of the RF Tx for various applications [2]. The state-of-the-art CMOS Txs proposed in the literature to improve Tx performance analyses are vital to understanding application-oriented RF Tx design techniques for further research.

Wireless communication systems have experienced rapid growth because of the advancement of CMOS technology [3], which meets the stringent cost constraints inherent in these applications [4]. In the RF regime, the benefits of silicon CMOS technology are its economic structure and that has the potential to be integrated with RF and silicon MOS-based mixed-signal circuitry [5]. CMOS technology also offers the prospect of integrating RF/digital/analog functions on a single chip in a low-cost manner [6]. For modern wireless devices, the CMOS Tx is a promising solution in satisfying the demand for low-power, low-cost designs; therefore, off-chip components, such as PIN diodes and metal-semiconductor field-effect transistors, are being increasingly replaced in RF systems [7], [8]. Implementation of the modern CMOS Tx in different wireless

CMOS Transmitters for 2.4-GHz RF Devices

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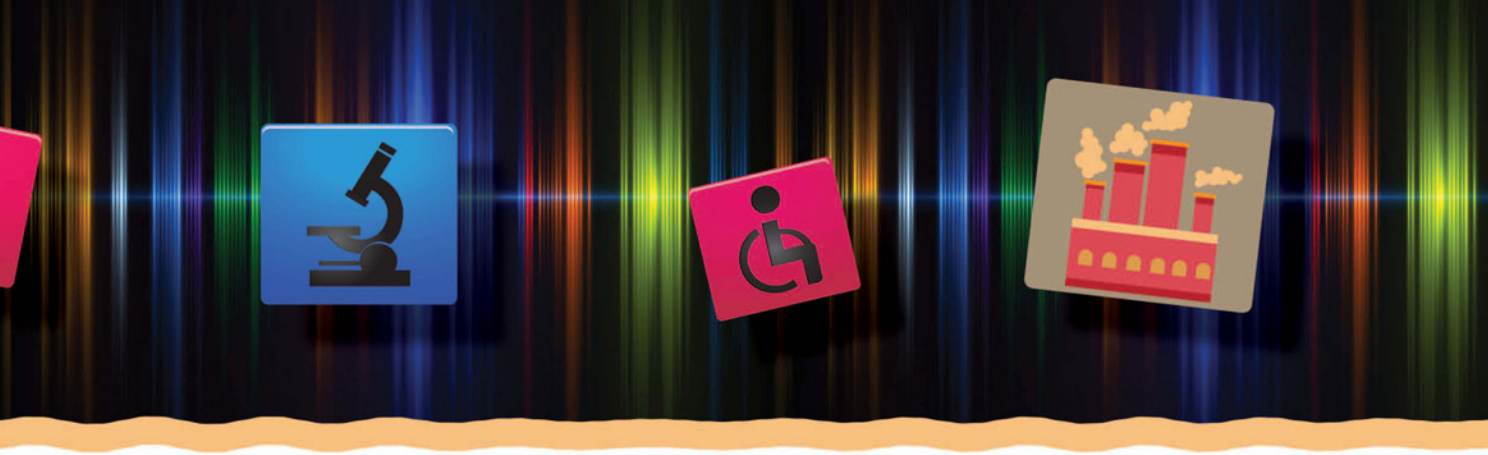

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communication devices has increased remarkably over the past decade because of the persistent scaling of CMOS technology. Low-power, low-cost, compact RF Txs are currently in demand for emerging short-range wireless communication applications [9], [10].

Wireless communication systems are increasingly sought after because of their portability and ease of access in addition to the widespread popularity of smartphones [11]–[13]. Predictions indicate that, in the next decade, mobile devices will become universal wireless terminals for multiservice systems. Shown in Figure 1 are current/recent trends in wireless communication systems as a result of the advancements in analog and RF circuit fabrication, signal processing, and large-scale integrated circuits.

A high-performance, compact Tx needs to be designed to meet this increased demand. The performance of a Tx is evaluated based on a few parameters, such as power consumption, linearity, noise figure, simple circuitry, gain, and chip size. Inevitable trade-offs exist among these factors, making Tx design in the 2.4-GHz industrial, science, and medical (ISM) band increasingly difficult [14], [15]. In CMOS downscaling, high-frequency RF devices experience constraints such as parasitic effects [16]. The comparatively smaller-length transistor creates larger flicker noise that contributes significantly to high phase noise (PN) [10]. As a result, the design of high-performance RF devices is difficult to achieve with CMOS technology.

IEEE standards 802.11 and 802.15.4 were established for low-rate wireless personal area networks that have an excessive consistency of nodes and a modest protocol. These standards are utilized for simple, low-cost, low-power, short-range wireless communication among portable and economical mobile devices in unregistered radio bands [17]. Given the advantages of the unlicensed 2.4-GHz band, the demand for wireless devices, such as RF identification (RFID), Bluetooth, ZigBee, and Wi-Fi, is continually increasing [18], [19]. The performance of the Tx contributes significantly to the overall performance of an RF device; therefore, a high-performance RF Tx must be designed. However, a few design configurations and specifications must be maintained in the design of high-performance RF Txs. In the case of short-distance communication for high-data-rate applications, IEEE standard protocols, such as IEEE 802.11b (Wi-Fi), need to maintain the basic requirement for bit error rate, i.e., better than 10^{-5}, and exhibit an acceptable PN of −101 dBc/Hz at 1-MHz offset from the carrier frequency [20]. To overcome such a rigid PN constraint, the CMOS Tx must consume a considerable amount of power, as described by different methodologies. A direct RF power oscillator topology-based 2.4-GHz Tx is suitable for low-data-rate ZigBee applications, in which the PN performance is more flexible than that in Bluetooth and Wi-Fi standard requirements [21].

The purpose of the wireless local area network (WLAN) is to provide fast web access at any time and wherever wired LANs are unavailable (and economically achievable) or when numerous supporters are scattered inside a moderately vast place, such as hotels and airports. Network protocols IEEE 802.11 DS and 802.11 FH, working at the 2.4-GHz ISM band, offer the highest data rate, i.e., 2 Mb/s, by implementing direct-sequence spread spectrum and frequency-hopping spread spectrum (FHSS) techniques, respectively [22]. The highest data rate that can be obtained for network protocol

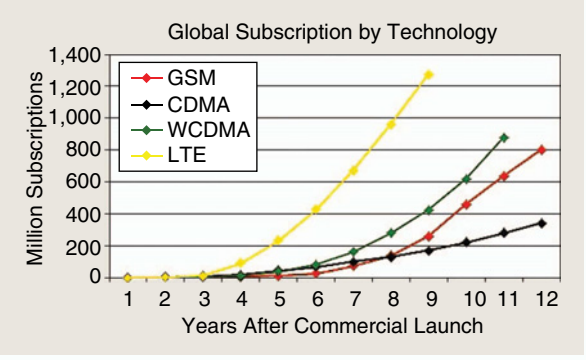

Figure 1. *The increasing demand for mobile networks in wireless communication systems [13]. GSM: global system for mobile communications; CDMA: code-division, multiple-access; WCDMA: wide-band code-division multiplexing access.*

TABLE 1. The protocol characteristics of IEEE Standard 802.11x.

802.11	802.11b	802.11fh	802.11g	802.11ds
Modulation	DSSS	FHSS	DSSS	DSSS
	DQPSK/DBPSK	DQPSK/DBPSK	DQPSK/DBPSK	DBPSK/DQPSK
	CCK	–	OFDM, CCK	–
	–	–	QAM/QPSK/BPSK	–
Frequency band	2.4 GHz[a]	2.4 GHz[a]	2.4 GHz[a]	2.4 GHz[a]
Channel bandwidth	22 MHz	1 MHz	16.25–22 MHz	22 MHz
Bit rate	1–11 mb/s	1–2 Mb/s	1–54 Mb/s	1–2 Mb/s

[a]: 2,402–2,480 MHz.

DSSS: direct-sequence spread spectrum; OFDM: orthogonal frequency-division multiplexing; CCK: complementary code keying; DQPSK: differential quaternary phase-shift keying; DBPSK: differential binary phase-shift keying; QAM: quadrature/amplitude modulation.

802.11b operating in the ISM band is 11 Mb/s; this is achieved using complementary code-keying modulation. At the 2.4-GHz ISM band, Bluetooth (IEEE 802.15.1) supports a data rate of 1 Mb/s by utilizing a 1-MHz channel implementing FHSS with Gaussian frequency-shift keying (GFSK) as the modulation. Table 1 presents the IEEE 802.11x protocol characteristics for short- and long-range wireless communication at the 2.4-GHz ISM band.

To overcome the difficulty of designing the Tx using CMOS, the Tx is employed in numerous potential applications scenarios, including home automation, RFID, industrial consumer electronics, sensor networks, biomedical devices, and automotive solutions [19], [21]. The goal of this article is to evaluate different design architectures of modern CMOS Txs for 2.4-GHz ISM band applications. Several comparisons are presented in analyzing the application-specific advantages and disadvantages of Txs according to their architecture and performance. We expect this comparative study to provide guidance for future research on 2.4-GHz RF devices.

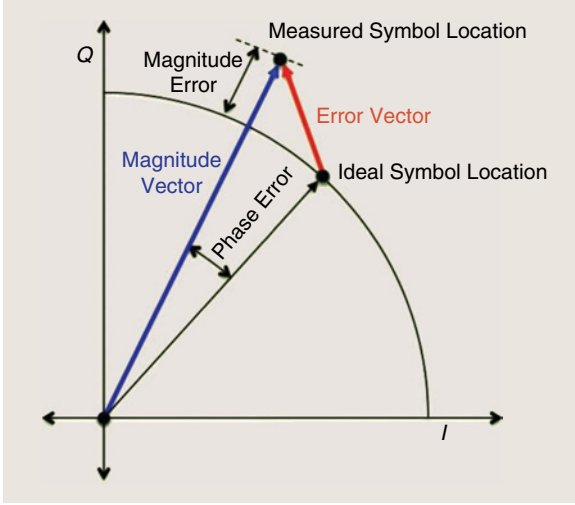

Figure 2. *The EVM measurement technique [29].*

Tx Performance Parameters

The performance of an RF Tx depends on several parameters. The key factors for the assessment of Tx performance are as follows:

1) Power consumption capacity is probably the most important performance parameter of an RF Tx. The increasing demand for portable operation must be addressed without consuming too much power to ensure the maximum run time of the device [23]. The very-large-scale-integration chip designer must overcome the limitations of power dissipation in portable electronic devices while maintaining the required design standard. Power dissipation can be reduced by applying a low-voltage source, reducing the device size, and using a small number of passive devices, such as inductors and capacitors. Passive devices generate additional noise sources that increase the devices' power consumption [24]. The power consumption of the Tx design also depends on the different architectures used; architectures with a small number of building blocks typically consume less power. For example, the quiescent power consumption of a frequency upconverter module can be reduced using adaptive biases. The maximum amplitude of the intermediate frequency (IF) and the switching frequency are responsible for the high power consumption and subsequent heat generation in active devices [25]. Therefore, during Tx design for portable RF devices, the most important issue is achieving a low-power design [19]; i.e., power consumption should be kept as low as possible.
2) Error vector magnitude (EVM) is the distance measurement of all constellation points from their ideal locations in a Tx, as described in Figure 2. All transmitted signals have constellation points in their ideal locations, but sometimes these locations vary because of imperfections, e.g., PN, low image-rejection ratio, and carrier leakage in the Tx

[26], [27]. EVM defines the quality of the transmitted signal [15] and determines whether it can be correctly recognized and demodulated. PN, spurious signals, and distortion negatively affect EVM, which inversely depends on Tx output power and power amplifier (PA) efficiency [28]. EVM can be improved; however, it is done so at the expense of reducing Tx output power and PA efficiency. Therefore, when designing a CMOS Tx, the EVM percentage (<35 dB) defined by IEEE 802.11 should be maintained. EVM can be described by the following relationship:

$$\mathrm{EVM\,(dB)} = \sqrt{\frac{\sum_{n=0}^{N-1} |\overrightarrow{e(n)}|^2}{\sum_{n=0}^{N-1} |\overrightarrow{r(n)}|^2}} \times 100\%, \tag{1}$$

where e(n) refers to the error vector between the real transmitted signal and the ideal transmitted signal, and r(n) stands for the real transmitted signal.

3) The adjacent-channel power ratio (ACPR) defines the quality of the transmitted signal [30] and represents the ratio between the adjacent-channel power signal and the root-mean-square error power of the transmitted signal in the main channel:

$$\mathrm{ACPR\,(dB)} = \mathrm{Po/P1}, \tag{2}$$

where P1 is the leaked power to the adjacent channel within the bandwidth of the signal power and Po is the power within the channel bandwidth. ACPR is related to the specific method of modulation, the accuracy of which is reduced by leakage power, that serves as interference to an adjacent channel. When the signal rate increases, the bandwidth also increases, and ACPR performance is degraded.

4) Linearity occurs when the output varies in a linear manner with respect to variations in the device input. The linearity performance requirement has become increasingly important in current RF communication structures. When linearity is improved, the Tx does not generate unwanted signals and rather produces an accurate copy of the input signal [31]. Linearity is often described using the value of a third-order intercept point (IP3). Approximately proportional to dc power consumption, IP3 normally improves with increasing dc power consumption; obtaining excessive linearity at low power is therefore remarkable. The graphical method exemplifies linearity by plotting the output power with respect to the input power at logarithmic scales and noting the location of the slope change [32]. Linearity can also be described by power-handling capacity, which is known as the *1-dB compression point* (*P1dB*) and measured by the input power that causes a drop of 1 dB in linear gain because of device saturation.

5) PN is a key element of the RF Tx because it can significantly affect the overall performance of the system. The power spectrum of the oscillation frequency in real oscillators, which extends into adjacent frequencies around that tone, is generally known as *PN* [33]. According to the classical Leeson's model for the linear oscillator, the PN $\Delta L(\Delta w)$ [33], [34] can be defined as

$$\begin{aligned} L(\Delta\omega) &= \frac{S_\theta(\Delta\omega)}{2} \\ &= 10\log\left[\left\{1+\frac{\omega_0^2}{(2\Delta\omega Q)^2}\right\}\left(1+\frac{\Delta\omega_{\frac{1}{f}}^3}{\Delta\omega}\right)\left(\frac{2FKT}{P_{DC}}\right)\right], \end{aligned} \tag{3}$$

where $\Delta\omega$ stands for the frequency offset from the carrier center frequency (ω_0), S_Φ stands for the power spectral density of PN, $\Delta\omega_{1/f}^3$ refers to the oscillator's flicker corner frequency, F is the noise factor, T is temperature, K is Boltzmann's constant, and P_{DC} is the dc power consumption of the oscillator. The PN performance of the Tx depends on several factors, such as high output frequency, high voltage gain, high temperature, Q-factor, number of voltage-control oscillator (VCO) delay stages, and loss properties of passive and active devices [35], [36]. PN can be reduced by selecting an appropriate delay-cell topology for rail-to-rail switching in VCOs with phase-locked loop (PLL). The PN performance of the overall Tx can be improved by further minimizing flicker noise upconversion in the tuning current and implementing a noise-free control path in the PLL's VCO. PN should be minimized for improved Tx performance.

6) Stability is another important issue in fully integrated CMOS Tx design. The incoming baseband signal is upconverted to an RF signal through frequency synthesis [37]. The stability of the output signal of a PLL significantly affects Tx performance; therefore, the design consideration for PLL is crucial for obtaining a stable RF signal. The loop bandwidth must be selected carefully so that the linear approximation is not violated (i.e., $\omega c < \omega REF$), thereby improving stability [38]–[40]. The key considerations in the design of frequency synthesizers (FSs) are abating the settling time and retaining high phase and frequency sensitivity so that the Tx operates at low power and maintains a compact die area [26], [41]. The rate at which the frequency of the output signal can be changed by an FS is defined by the settling time [42]. The settling time of the FS is not clearly defined in IEEE 802.11, but it can be derived from the correlation of time-slot length and packet length as follows:

Power dissipation can be reduced by applying a low-voltage source, reducing the device size, and using a small number of passive devices, such as inductors and capacitors.

$$T_{down}(\mu s) = T_{slot} - T_{pkt}, \quad (4)$$

where T_{slot} refers to time-slot length, T_{pkt} refers to packet length, and T_{down} is the downtime between two consecutive time slots.

To design an efficient 2.4-GHz RF Tx, the performance of these parameters must be improved. The Tx should be designed in such a manner that it has low power consumption, low PN, good EVM and ACPR value, good stability, short settling time, and high linearity.

Growth of CMOS 2.4-GHz Txs

The rapid growth of 2.4-GHz ISM-band devices demands low-cost, low-power solutions. Despite continued advances in CMOS, achieving this goal remains challenging for system-on-chip designers [21]. Tx design specifications include current consumption, output power, leakage current, linearity, ACPR, and EVM. Figure 3 shows the basic block diagram of a 2.4-GHz RF Tx. The Tx often consists of a digital-to-analog converter (DAC), a low-pass filter (LPF), a variable-gain amplifier (VGA), a local oscillator (LO), an upconversion mixer, a transimpedence driver amplifier, and a PA.

The DAC converts the digital signal from the baseband to an analog signal and passes it to the LPF for filtering. The LPF then removes the image that accompanies the analog signal and sends it to the VGA, where the signal is variably amplified. The mixer combines the analog and LO signals to upconvert them to an RF signal. The signal is then amplified and sent to the antenna. Several modifications have been performed on this basic architecture to meet application-based Tx requirements. Literature reviews reveal a few design configurations for CMOS Txs, such as superheterodyne, two step-up, direct conversion (DCT) or zero-IF, and PLL-based Txs. This article describes advances made in these Txs with respect to their circuit architecture and performance.

Superheterodyne Tx

The superheterodyne Tx architecture has become one of the leading designs for high-frequency RF Txs; a typical block diagram is shown in Figure 4. The Tx is composed of a DAC, an LPF, an LO, a channel-selection filter, an image-rejection filter, a PA, and a band pass filter (BPF). The advantages of the RF superheterodyne Tx are low LO leakage and a high-quality transmitted signal [44]. However, the architecture consists of complex circuitry and consumes high power because of additional filters, such as those used for image rejection.

Only one channel is upconverted during transmission in the superheterodyne Tx, and the image channel is prevented from being superimposed onto the desired channel by a high-Q, off-chip image-rejection filter. An image-rejection filter is required to remove the created image from the digital-to-analog signal conversion. The PLL and quadrature VCO (QVCO) are required for upconversion to produce in-phase/quadrature (I/Q) components. Given that the Tx power channel is radiated by the PA and gradually amplified to the antenna,

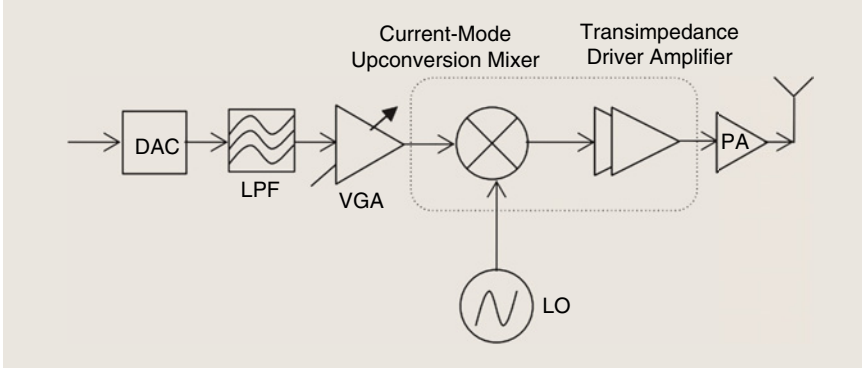

Figure 3. *The basic block diagram of a 2.4-GHz RF Tx [44].*

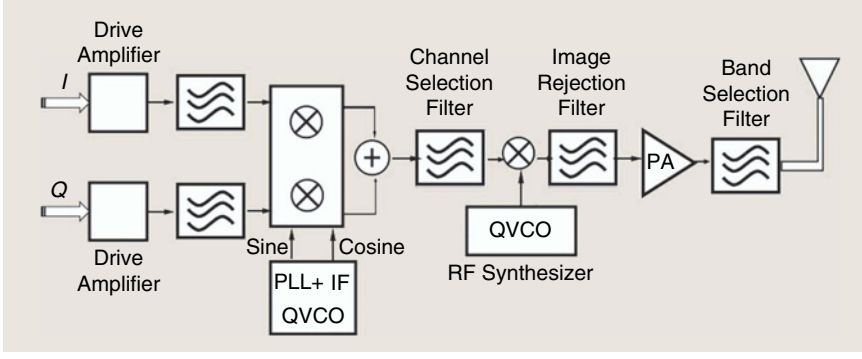

Figure 4. *The basic block diagram of a superheterodyne Tx [48].QVCO: quadrature voltage control oscillator. IF: intermediate frequency; Q: quadrature-phase; I: in-phase.*

the overall linearity performance of the Tx depends on the PA. The high power consumption and low integration level for on-/off-chip buffering along with noise problems and the shuffle of dc offset are the main concerns in the superheterodyne architecture [45], [46].

As examples, Chu et al. presented a superheterodyne Tx for an RF front-end base station to be utilized in Time Division Long-Term Evolution (TD-LTE) communication [30]. The proposed Tx consists of two digital attenuators, a modulator, several filters, an upconverter, and a PA. Decent PN performance was achieved by applying two PLLs. The RF LO frequency performs digital control and determines the number of digital attenuators and the Tx working mode. In this design, EVM performance is improved, i.e., by $<8.2\%$ under the condition of 100-M symbol per second (sps) and $<1.8\%$ under the condition of 10-M sps in the signal test of 16-quadrature amplitude modulation (QAM) [30]. The evaluated transmission power is 0.2 W, and the intermodulation distortion from the third order of a circuit value is below -40 dB. The disadvantages of this architecture are gain flatness and high LO leakage, which were later addressed by Hsieh et al. in [48]. To prevent out-of-band interference effectively and to achieve good selectivity in RF communication, the superheterodyne structure is adopted in both the downlink and uplink of the base station.

Hsieh et al. described the implementation and design of a low-cost CMOS transceiver based on the superheterodyne architecture for IEEE 802.11g's RF front end [48]. The current trend in the WLAN market is increased data rate [49], and the IEEE 802.11g WLAN standard can support data rates up to 54 Mb/s by utilizing orthogonal frequency-division multiplexing along with the proposed design, which is aimed at achieving high data-rate compatibility. The Tx was designed using an auto-tuning mechanism that confined the gain mismatch to within 0.1 dB and the phase mismatch to within 1°. The VGA determines the Tx output power range, which fluctuates between -23 and 2 dBm. An external 40-MHz crystal oscillator was used to generate a 1-MHz reference frequency to operate an integer-N PLL. The RF VCO frequency was tuned to 280 MHz by incorporating three additional capacitor arrays in parallel into the tank circuit. The local leakage power level was converted into dc voltage by a peak detector on the IF output, which was amplified by the subsequent gain cell and then applied to a sample-and-hold (S/H) comparator, as shown in Figure 5. The integrated S/H comparator provides information on dc-offset polarity, which usually occurs along the I path. The upconversion mixer combines and converts the IF and VCO frequency to RF.

The proposed Tx achieved gain control of 25 dB at a supply voltage of 2.7–3.3 V; the supply current in Tx mode was 120 mA, which is considered high power consumption [48]. Although the design has significant gain control at 1-MHz offset, the IF and RF VCOs suffer from PN of -120 and -116 dBc/Hz, respectively. However, the design demonstrates high nonlinearity, which was later improved on by Chien et al [50]. The proposed Tx was implemented in a 0.25-μm CMOS process, and the Tx chip delivered a 7-dBm Tx output-gain compression.

Chien et al. proposed another superheterodyne Tx design to complete a physical layer chipset for IEEE 802.11b; the Tx is composed of a baseband processor and a fully integrated CMOS transceiver [50]. In the Tx path, the baseband signal is upconverted in two steps. The dc-offset is removed by calibrating the Tx path between the IF mixer and the baseband to minimize LO leakage, as illustrated in Figure 6. Unlike in a DCT topology, VCO pulling is minimized by the separation of the two LO frequencies. The linearity of the input stage is improved by implementing resistor degeneration in combination with operational amplifier

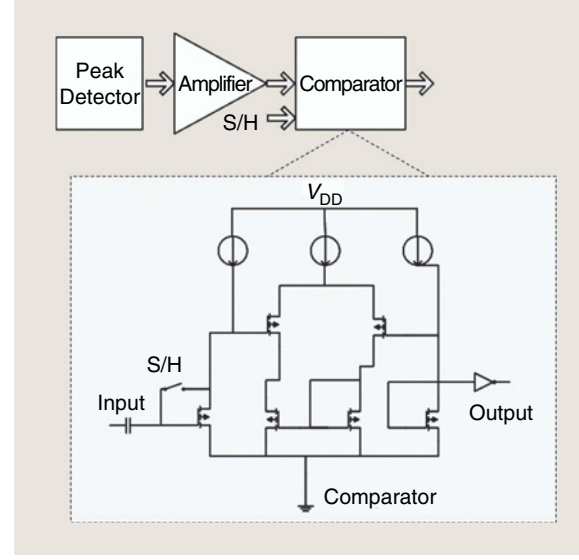

Figure 5. *The architecture of a Tx detector and comparator [49].*

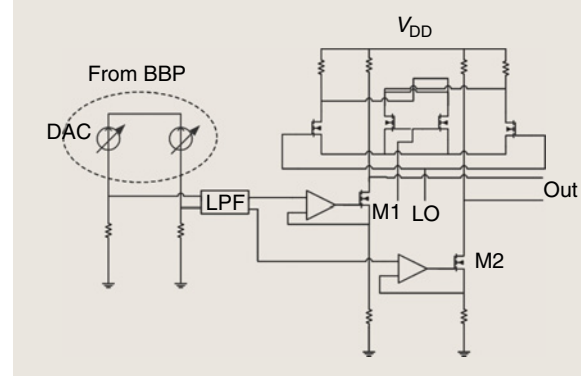

Figure 6. *The Tx baseband-offset-cancellation method [51]. BBP: baseband processor.*

TABLE 2. A performance comparison of the different superheterodyne Txs.

Reference Number and Year	CMOS Process	Supply Voltage (V)	Tx Output Power (dBm)	EVM (%)	Noise Figure (dBc/Hz)	Gain (dB)	Applications	Modulation	Advantages	Disadvantages
[30] (2013)	–	–	–	<8.2%	–	60	TD-LTEA communications	16-QAM	Very minimal EVM (<1.85% at 10-M sps, <8.2% at 100° M sps) Minimal PN Satisfactory performance of ACPR (−42.1 at 10-M sps, −31.1 at 100-M sps) Good accuracy of modulation and demodulation	High LO leakage Gain flatness EVM value decreases when the sample rate increases
[49] (2005)	0.25-μm CMOS	2.7	−23	−3.2%	−116	24	IEEE Standard 802.11g	OFDM	Reduced PN mismatch Reduced gain noise mismatch Improved Tx output gain compression (7 dBm)	I/Q gain mismatch High PN of −116 dBc/Hz (RF) and −120 dBc/Hz (VCO) at a 1-MHz offset
[51] (2003)	0.25-μm CMOS	2.5	20	–	−110	74	IEEE Standard 802.11b	DQPSK	Can maintain a constant output power because of the power control loop Small die size Minimum LO leakage Improved linearity	The modulated chip-rate Tx signal is up-sampled eight times, which causes high EVM values Complex circuitry High PN

OFDM: orthogonal frequency-division multiplexing; DQPSK: differential quaternary phase-shift keying.

(op-amp) feedback in the Tx's IF mixer. Reliable device performance is ensured by integrating cascode transistors.

In this design, a fully differential, three-stage amplifier is used to achieve optimal power consumption and linearity, and each stage of the PA can be controlled independently. The synthesizer achieves a PN of −110 dBc/Hz at 1-MHz offset and locks the VCO frequency to the reference frequency of 1 MHz. The average output power of +20 dBm at the antenna port is achieved with a single 2.5-V power supply [50].

The IF interface is adopted for the base-station RF front end, and these interfaces demodulate the two IF signals in [30]. The quadrature and phase signals are not strictly orthogonal, and the IF interface has a higher modulation accuracy compared with the baseband interface. In [48], auto-I/Q calibration control logic is performed. This process changes 1 b in the Tx input buffer DAC to create an extra dc signal along the I path. Test vectors are implemented in various time slots of the Tx input, and the I/Q path-gain mismatch creates different signal power levels that appear in the modulator output. The upconversion mixer receives a 5-MHz quadrature signal from the 40-MHz reference-frequency clock divided by 8. The LO leakage is minimized in [50], creating a calibration between the baseband and IF mixer along the Tx path. The external component variation and output power-over process are maintained constantly by a power-control loop that controls the output level to match a predefined reference. A performance comparison of superheterodyne Txs is presented in Table 2.

Chu et al.'s [30] superheterodyne architecture, shown in Table 2, is the best among the compared structures in terms of EVM and ACPR performance. At 10-M sps, EVM is <1.8% and ACPR is 42.1, both of which help propagate a decent transmitted signal. Chien et al. [50] improved linearity by maintaining minimum LO leakage. Compact die size and constant output power are also maintained because a new power-control loop is implemented; however, this architecture exhibits complex circuitry and high PN because of the extra power-control loop.

Two-Step-Up/Dual-Conversion Tx

The two-step-up design architecture is convenient because of the easy frequency synthesis in the PLL. This architecture is also referred to as

dual conversion, because of its frequency synthesis in two steps, and offers many advantages, the most important of which is the extremely wide gain-control range that effectively solves substrate isolation problems. Furthermore, the architecture is relatively insensitive to LO leakage and possesses good ACPR [51]. It does, however, produce high PN and nonlinearity. The die is also relatively larger than that of others because of the extra functional module and circuit complexity. This architecture can be designed through one of the following two schemes.

1) *Scheme 1*: Before digital-to-analog conversion, the desired channel is digitally translated to high frequency in such a manner that the low-frequency interference of the LPF and DAC is disregarded through ac coupling. At the same time, the transmission of dc-to-LO mixing is avoided. In this case, the required conversion rate of the DAC and LPF bandwidth must be increased. A complex filter can be used to reject the image because of I/Q mismatch, resulting in improved spectrum purity. Figure 7(a) shows a block diagram of scheme 1.
2) *Scheme 2*: The analog baseband-to-IF upconverter is placed between the complex filter and the DAC. This placement delivers double image rejection and allows capacitive coupling between the complex filter and the upconverter. The scheme also allows independent dc biasing for each functional block. Another advantage of this scheme is its low LO leakage. However, for mixing, filtering, and frequency synthesis, it consumes a large chip area. Figure 7(b) shows the scheme 2 design method.

Mak et al. presented a design technique for a two-step-up Tx that can handle the unwanted image signal produced during RF-to-IF conversion and vice versa [53]. The goal of this technique is to reduce the locking time and PN requirements of the PLL. The dual-band operation is performed with 450- and 1,350-MHz LO frequencies. In the two-step-up mode, the effect of LO–LO self-modulation is abated by setting the first IF to half channel spacing. Additionally, this technique maintains the balance of design trade-offs between low-frequency noise elimination and image rejection. The design technique also reduces the difficulties by the LO and FS through channel-selection partitioning. The main disadvantages of this proposed design are the DAC's production of multiple harmonic signals and unwanted image signals during frequency synthesis. These unwanted image signal and multiple harmonic signal problems can be removed by adopting Leung et al.'s method in [54], thus ensuring a high-quality signal.

A highly integrated, low-power two-step-up Tx circuit implemented in a 0.25-μm silicon-germanium bipolar-junction-transistor CMOS process for wide-band code-division-multiple-access (CDMA) handset applications was reported by Leung et al. [54]. The Tx design focuses on low power consumption and a high level of integration. The Tx maintains good waveform quality (as measured by ACPR and EVM) and reduced emission to prevent desensitizing. The high power consumption and complex filtering problems typically related to digital IF interface are mitigated by implementing an optimum frequency plan and a high-speed DAC. Adaptive biases are designed to reduce the quiescent power consumption of the upconversion mixer and RF amplifier and provide a current boost when required. The Tx integrates a low-power, high-speed DAC to drive a dominantly capacitive load. The main advantage of the designed Tx is its very low EVM value, which is only 1%, and its ACPR values

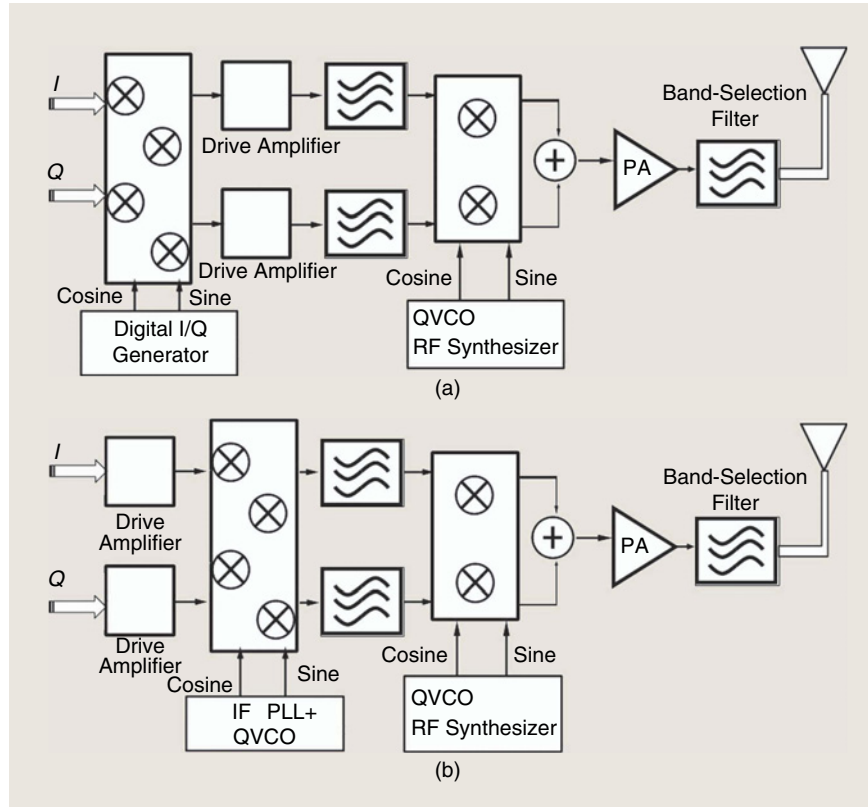

Figure 7. *The basic block diagram of a two-step-up Tx for (a) scheme 1 and (b) scheme 2 [48], [53].*

The high power consumption and complex filtering problems typically related to digital IF interface are mitigated by implementing an optimum frequency plan and a high-speed DAC.

of −42 (at 5 MHz) and −51 (at 10 MHz). The Tx dissipates 180 mW at a 3-V power supply for a maximum output power of +5 dBm; the value decreases to 120 mW at the time of power back-off [54]. However, this design suffers from high PN of −38.6 (dBm/5 MHz) [54], which was reduced by Kulge et al. [55] using an inductor/capacitor (LC) tank.

Kwon et al. used a dual-conversion architecture to design a 2.4-GHz RF Tx with good ACPR performance and minimal power consumption; the Tx is shown in Figure 8 [31]. The architecture consists of a 4-b current-steering DAC, a current amplifier-based upconversion mixer, a current-mode amplifier, and a driver amplifier. The current-mode filter is a combination of a current-mirror and a second-order LPF and also implements dual-conversion I/Q modulation.

Multiple V–I conversions create nonlinearity in the system, which is reduced by executing a current amplifier-based upconversion mixer, as demonstrated in Figure 9. The current-mirror amplifier performs the amplification and upconversion of the baseband signal to a 2.4-GHz signal by a double-balanced mixer using a 1.92-GHz integer-N PLL-based LO. The unwanted image signal in this design is reduced by the LC tank load.

The first IF has been designed so that the image appears out of the Tx band [54]. This phenomenon occurs only when the clock rate is 250–260 MHz and $f_{IF} = f_{clk}/4$ is executed for the quadrature modulator. Consequently, the quadrature LO will accept values of +1, 0, or −1, and multiplication is a simple sign-bit flipping/zeroing. To generate 480 MHz and 1.92 GHz, respectively, LO signals maintaining a 5-MHz channel, along with a spacing-integer-N FS derived from a 16-MHz crystal with (+/−) 20 pulse-position modulation (PPM) accuracy, are implemented [31]. The beamwidth (gain) is digitally scaled using a capacitor bank [56] in the feedback capacitors [53]. The 2-b digital controller is designed to set up the filter's center frequency. This controller organizes the MOS array of switches such that it either switches the differential terminals to center the filter at ω_c (i.e., tunable center frequency) or it connects the I/Q cross-feedback resistors to the common-mode voltage to enter the filter at dc. A performance

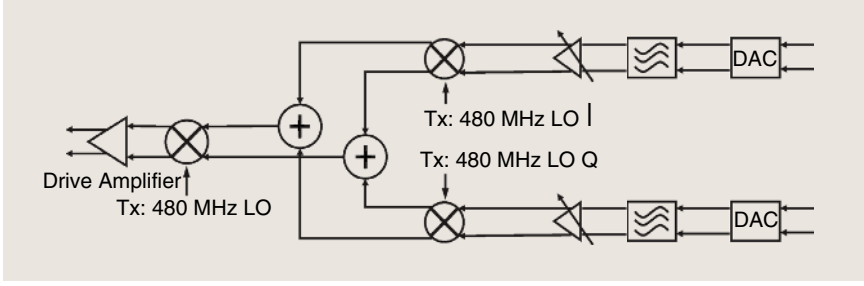

Figure 8. *A fully integrated 2.4-GHz two-step-up Tx [31].*

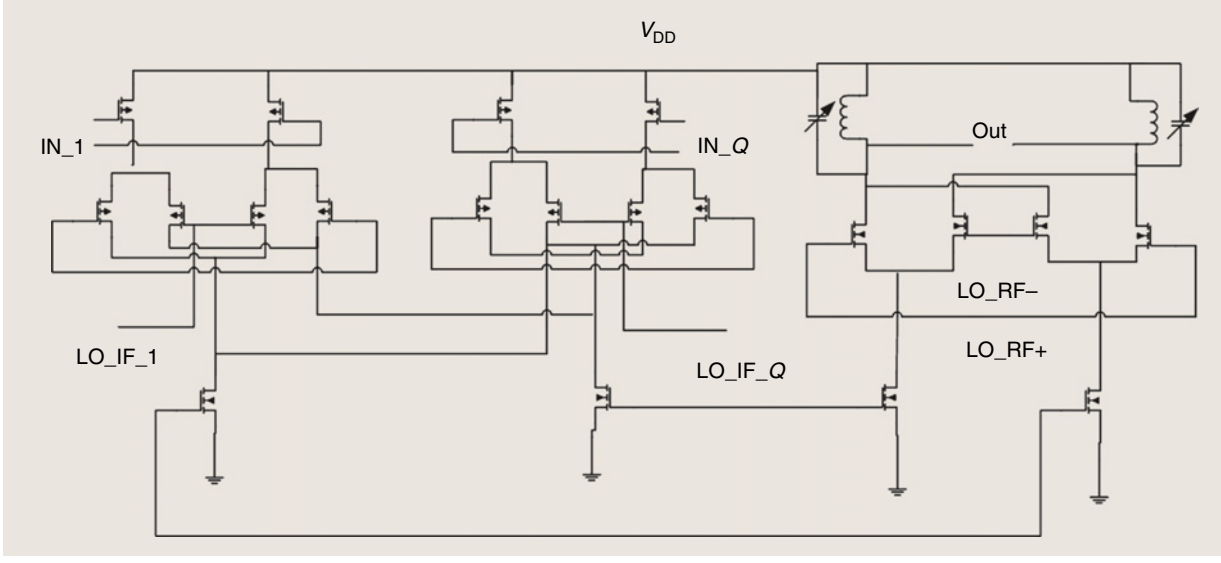

Figure 9. *The upconversion mixer with a current-mirror amplifier [31].*

comparison of various two-step-up Txs is presented in Table 3, which shows the two-step-up Tx designs proposed by Leung et al. [54], Mak et al. [53], and Kwon et al. [31].

The architecture proposed by Leung et al. [54] achieves good signal quality and demonstrates the best EVM performance (1%) fabricated in 0.25-μm silicon germanium bipolar-junction-transistor CMOS (BiCMOS). Mak et al. [53] improved the LO for easy frequency synthesis to obtain a stable output signal and low PN. However, the DAC produces multiple harmonic signals that reduce signal purity [53]. Kwon et al. [31] designed a Tx integrated circuit (IC) with high linearity due to a small number of V–I conversions in the mixer.

Direct-Conversion Tx

The DCT is a widely used architecture of 2.4-GHz RF Tx design. DCT is also known as a *zero-IF architecture* and *direct-upconversion architecture*. The main advantages of the DCT topology are minimal dc-offset noise [57] and simple design. As a result, the power consumption and die area are generally very low. A DCT usually consists of a DAC, an LPF, an upconversion mixer, a driver amplifier (DA), and an LO, as shown in Figure 10.

Nguyen et al. proposed a basic DCT incorporated with an I/Q upconversion mixer along with a single-sided, two-stage DA, as presented in Figure 11 [58]. The power consumption is confined to 9.72 mW by adopting a conventional passive mixer that does not dissipate dc current. The single-sided, two-stage DA improves stability by implementing the inductive-load cascode topology with a feedback resistor and capacitor in the output stage. The linearity of the Tx is also improved by using a folded cascode topology in the gain stage. The output stage employs a folded cascode topology that improves linearity while allowing minimal high-voltage headroom. Stability is improved in the gain state by incorporating an inductive-load cascode technique with the feedback resistor. The offset quaternary phase-shift keying (OQPSK) modulation scheme, which is highly flexible for cost-effective Txs, is used. However, this design suffers from poor sideband rejection and extremely high LO leakage (~30 dB), which was minimized by Sacchi et al. using a quadrature Gilbert mixer technique [59]. The input voltage is boosted by an additional capacitor between the two stages; this, in turn, helps reduce the overall power consumption. The EVM achieved with this architecture is <35% [58].

Seong et al. significantly improved the linearity performance of a DCT by implementing a linear current-mirror amplifier in the upconversion mixer stage [57]. The EVM value was also improved to 8.4%. The achieved gain-control range was 18 dB, and the gain step was 6 dB. The OQPSK modulation scheme (with

TABLE 3. A performance comparison of different two-step-up Txs.

Reference Number and Year	Supply Voltage (V)	Power Consumed (mW)	Tx Output Power	Noise Figure	Gain (dB)	Applications	Modulation	Process	Advantages	Disadvantages
[55] (2004)	3	180	5 dBm	38.6 (dBm/5 MHz)	76	Wide-band CDMA	Dual conversion I/Q	0.25 μm SiGe BiCMOS	Good signal quality (EVM of 1%, ACPR of −42 (at 5 MHz) Minimized spurious emission	High PN High power consumption
[54] (2005)	–	–	–	–	60	Bluetooth	GFSK	0.35 μm CMOS	Relaxes FS and LO design difficulties Relaxes PN LO pulling susceptibility is low	Creates unwanted images DAC produces multiple harmonic signals
[31] (2006)	1.8	42	−24 dBm	−100 dBc at 1 mhz	–	IEEE 802.15.4	Dual conversion I/Q	0.18 μm CMOS	Low power consumption Improved linearity	Unwanted sideband is produced at output Amplitude mismatch

SiGe BiCMOS: silicon-germanium bipolar-junction-transistor complementary–metal-oxidesemiconductor.

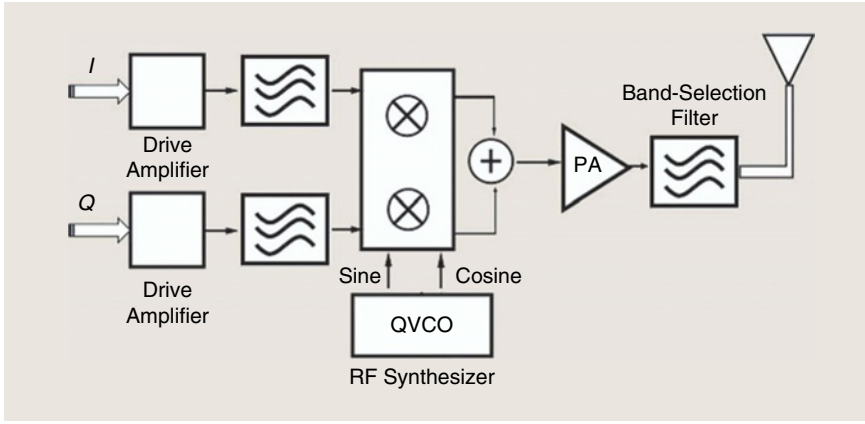

Figure 10. *The basic block diagram of the DCT [32].*

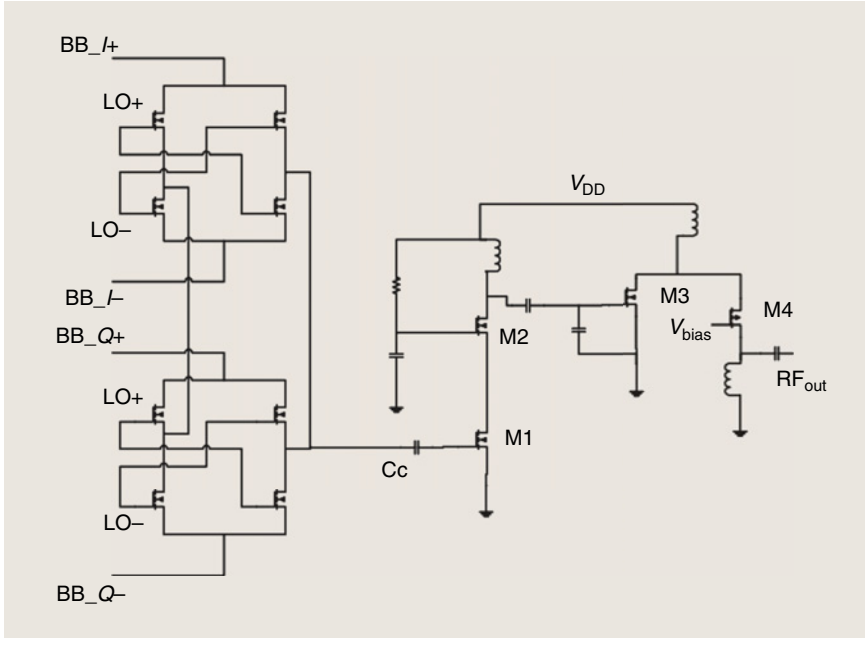

Figure 11. *The schematic of an RF DCT Tx proposed by Nguyen et al. [58]. Cc: connecting capacitor.*

half-sine-wave forming) and the frequency-mixing technique were used to generate the required LO signals. As a result, the output power was improved, and current consumption was minimized. The design, however, could not overcome the high LO leakage in the Tx.

To further improve linearity, Nam et al. proposed a technique that employs a vertical negative-positive-negative (V-NPN) current mirror [60]. This current mirror enables the V–I converters to be eliminated in the upconversion mixer. The output current from the DAC is mirrored through the V-NPN current mirror. A V-NPN input stage with a current-mirror upconversion mixer was implemented, as depicted in Figure 12 [60]. Satisfactory linearity performance was achieved by applying this technique. Differential phases are used in this topology, which reduces second-order harmonics. Power consumption is reduced using a first-order RC LPF. This topology leads to a high ACPR value and minimal current consumption at the expense of reduced output power. A block diagram of the proposed architecture is presented in Figure 13.

Kwon et al. proposed a DCT architecture (Figure 14) that maximizes the output power of the Tx by utilizing the common source technique in the DA [61]. This architecture is composed of a 6-b, current-steering DAC; a quadrature Gilbert cell upconversion mixer; a DA; and a "leapfrog" second-order LPF. The DAC uses a current cell–matrix stage in the architecture. The DAC is composed of three decoders, a 4 × 4 current cell controlled by the most significant bit, and a 4-b, 2 × 2 current cell controlled by the least significant bit. The 2-b, second-order Butterworth-active RC LPF used reduces the clock harmonic component from the DAC. LO leakage is minimized using a quadrature Gilbert mixer topology [62] in the upconversion mixer. This architecture maximizes the Tx output power but exhibits increased power consumption and decreased EVM performance because of high PN.

Choi et al. created a low-voltage DCT design (Figure 15) by implementing a current-mode circuit to improve power consumption and linearity performance simultaneously during the 130-nm CMOS process [63]. The Tx dissipates only 10.2 mW of power at 1.2-V single-supply voltage [63]. A current mirror composed of a common-source, single-transistor amplifier and a diode-allied transistor is utilized. The unwanted high-frequency signal is attenuated by inserting an RC filter between two transistors, which make up the current mirror. The harmonic signals produced by the DAC are removed by implementing an RC-type LPF. Good isolation between the output and input ports is achieved by designing a cascaded DA.

Darabi et al. designed a direct upconversion Tx for Bluetooth and IEEE 802.11b applications [64]; a fractional N-FS was used to perform frequency synthesis. Two

fifth-order channel-selection filters were utilized in this architecture. The first 7.5-MHz LPF centered at dc was implemented for IEEE 802.11b, and the second 1-MHz LPF centered at 2 MHz was implemented for Bluetooth. The proposed design generates a positive dc offset, which is marginally removed by using an offset cancellation loop.

Huang et al. proposed a fully integrated, commercial TD LTE triband Tx based on a DCT architecture [9]. The carrier leakage was reduced to −40 dBc over an 86-dB gain-control range by implementing novel carrier-leakage calibration and proper gain allocation. The Tx consumes high power of 183 mW because of the implemented off-chip PA with constant gain, but it helps obtain 4-dBm Tx output power [9].

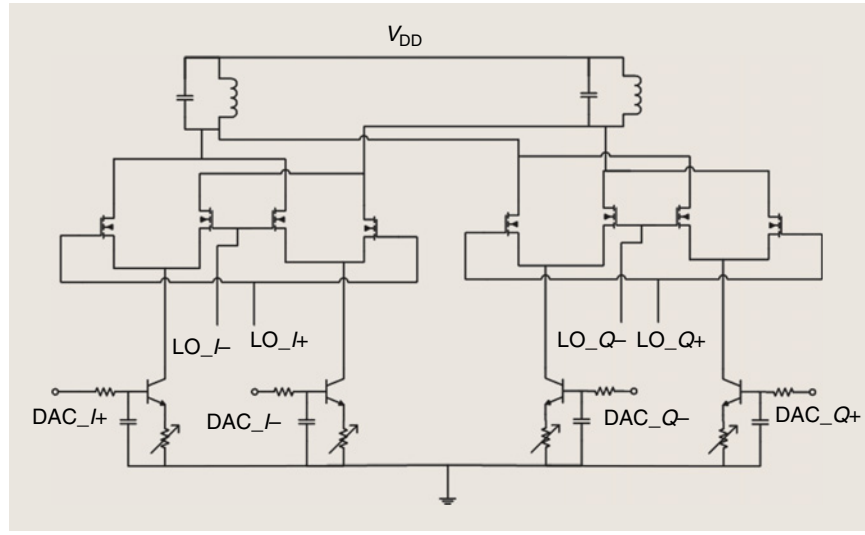

Figure 12. *A V-NPN current-mirror upconversion mixer [61].*

Although power consumption is reduced to 9.7 mW by Nguyen et al. [58], this architecture generates glitches by the switching operation [65]. The source of the glitches is the coupling of the switching-control signals to the DAC output lines through the parasitic gate-drain capacitance of the switching transistors. When the number of switching transistors is large, significant glitches occur at the DAC output, which cause distortion of the input signal. The glitch problem can be solved by operating the switching transistors within the linear area and attempting to compensate for the signal feedthrough by connecting parallel dummy transistors driven by the complementary control signals. The drain of the switching transistor can be isolated from the output lines by integrating cascaded transistors to minimize the feedthrough to the output lines.

The glitch problem is reduced in [58] by employing a transistor along with the switching transistor. High gain-control range is achieved by designing a 2-b controlled VGA in front of the upconversion mixer [57]. The VGA circuit is designed using a simple switched-resistor op-amp to control the gain. The 2-b control is implemented for LC tuning. In [60], the incoming 16-MHz input and the data in the DAC are transformed into differential data with internal inverters. A V-NPN diode-connected load is used for current mirroring. Employing a resistor

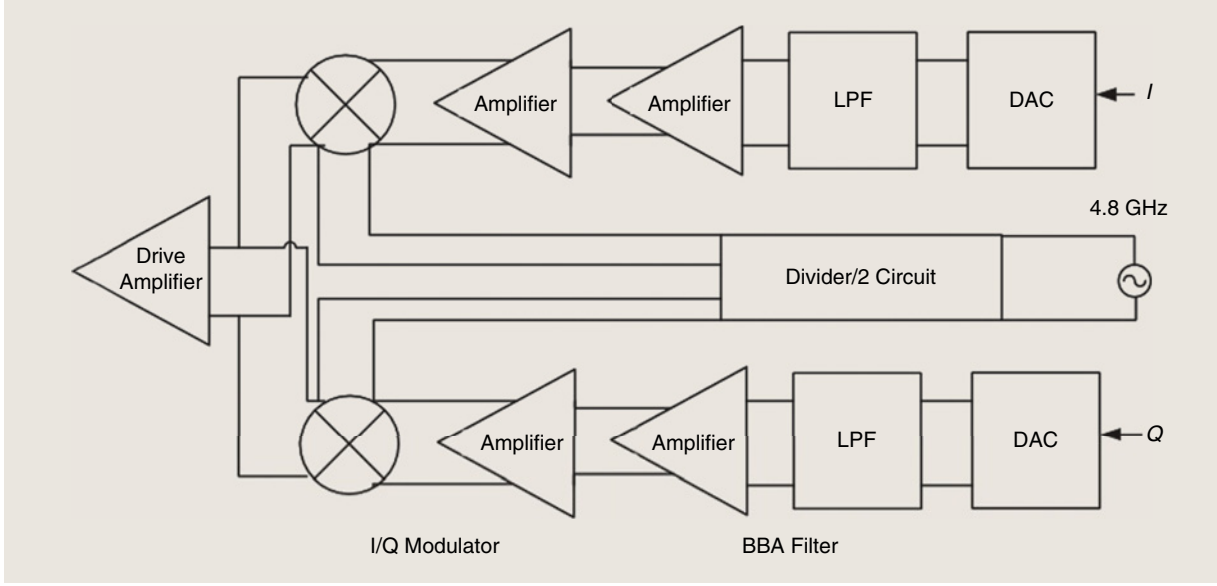

Figure 13. *A block diagram of the DCT proposed by Nam et al. [61].*

When the number of switching transistors is large, significant glitches occur at the DAC output, which cause distortion of the input signal.

below the input V-NPN load reduces the current mismatch in [66]. Kwon et al. [61] utilized the input block as a replica circuit integrated with the feedback amplifier to obtain high linearity (from the low supply voltage) and a large swing. In [9], the odd and even harmonics are removed by implementing an inductive output load and differential structure, respectively. The short switching time prevents excessive loss in the mixer switches, and complete switching is achieved by simultaneously increasing the switch width/length ratio and LO amplitude [9]. Table 4 shows a performance comparison of different DCT structures designed for different wireless communication devices in the 2.4-GHz ISM band.

As the table shows, a low power consumption of 9.72 mW, excluding the PLL, is achieved by Nguyen et al.'s architecture [58], although it suffers from extremely high LO leakage. LO leakage is minimized in Kwon et al.'s architecture [61], but at the expense of higher power consumption. Eo et al. [57], Nam et al. [60], and Choi et al. [67] improved Tx linearity performance by implementing a linear current-mirror amplifier in the upconversion mixer stage and using V-NPN techniques. However, the architecture in [60] creates an amplitude mismatch in the LO that affects EVM performance. Chai et al. [9] achieved high gain-control range at the expense of high PN and a high power consumption of 183 mW.

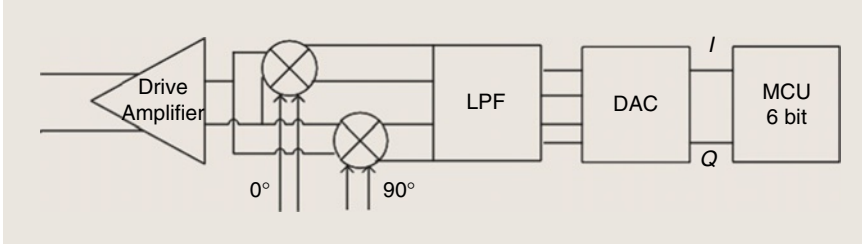

Figure 14. *A block diagram of the Tx proposed by Kwon et al. [62].*

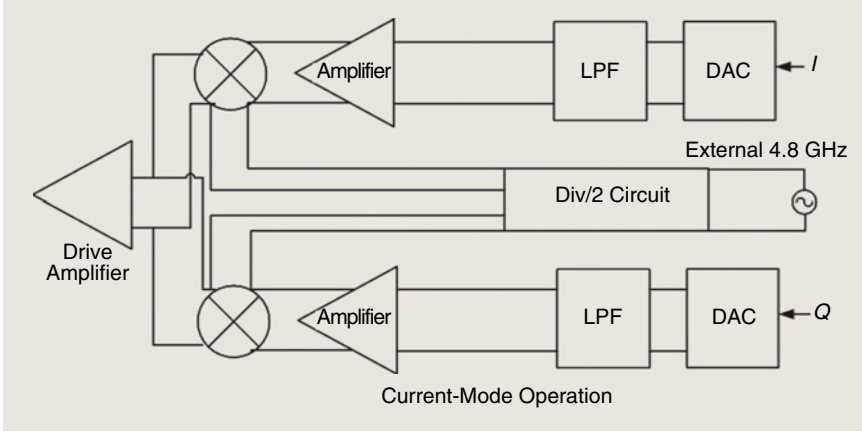

Figure 15. *The 2.4-GHz DCT proposed by Choi et al. [64].*

PLL-Based Tx

The PLL-based Tx is another popular architecture for 2.4-GHz RF Tx design. The main advantages of this design method are high output power, low power consumption, and high linearity [19]. However, this architecture presents several disadvantages, such as high PN and high dc-offset noise. An important issue in PLL-based Tx design is reducing the lock-in time of the PLL because a short lock-in time reduces Tx energy consumption. To achieve a fast lock, the system clock is deactivated, thereby lowering the architecture's energy consumption [7]. The lock-in time of a PLL can be derived from

$$T_{\text{lock-in}} = \frac{1}{\zeta \omega n} \ln\left(\frac{\Delta F}{\varepsilon\sqrt{1-\zeta^2}}\right), \tag{5}$$

where ΔF refers to the initial frequency error, ε stands for the standard frequency error, ζ is the damping factor, and ω_n is the natural frequency of a PLL. Lock-in time mainly depends on the initial frequency error ΔF; therefore, lock-in time is significantly reduced when ΔF is small.

Apart from reducing lock-in time in PLL designs, another fundamental issue in PLL-based Tx designs is the frequency synthesis required to obtain a stable RF signal as an output. The entire FS system is designed to guarantee the accuracy of the output frequency under any condition. It continuously converts the frequency of a controlled oscillator until it matches the input signals in both frequency and phase [38], [39].

Chen et al. proposed an energy-efficient, PLL-based 2.4-GHz Tx fabricated using a 0.18-μm CMOS process [67]. A novel twin-VCO transmission scheme was implemented, and the technique achieved high data-rate (18 Mb/s) transmission with steady carrier frequency. The proposed twin VCO operates in transmit mode with a high transmission data rate, which reduces the loop bandwidth of the PLL and produces a quadrature carrier for the receiver. As shown in Figure 16, throughout

the transmit mode, the twin VCO is decoupled.

Figure 17 shows a schematic of the proposed twin VCO. The recommended Tx overcomes the transmission data-rate constraint by adopting a closed-loop modulation architecture and achieves <21 PPM frequency precision at 2.4-GHz carrier frequency [67]. The integrated frequency-presetting system reduces the lock-in time to <7 μs of the PLL along with a minimized VCO gain variation. The designed Tx expands 11.6 mW for 18-Mb/s modulation to obtain 0 dBm of output power and accomplishes energy efficiency under 0.64 nJ/bit. Furthermore, the designed chip covers a die area of only 1 × 1.5 mm, which is much smaller than that covered by other architectures [67]. However, this recommended architecture suffers from high PN of −111 dBc/Hz at a 1-MHz offset, which was solved efficiently by Zhang et al. in [68].

Zhang et al. proposed a PLL-based, energy-efficient 2.4-GHz RF Tx (Figure 18) for wireless medical applications [68], which solved the PN problems in [67]. The reported Tx is composed of a class-B PA, a PLL synthesizer associated with a direct frequency-presetting method, nonvolatile memory (NVM), and a digital processor. The frequency-predetermining technique can precisely preset the carrier frequency of the VCO and scale back the lock-in time of the PLL synthesizer, further expanding the data rate of the communication system at low power consumption. The calibration and presetting data are stored in the NVM; as a result, the repetitive calibration process of the Tx is avoided, and energy is saved in practical applications. Optimum energy efficiency and reduced PN are achieved in this design by combining PLL-based

TABLE 4. A performance comparison of different DCTs.

Reference Number and Year	Supply Voltge (V)	Power Consumed (mW)	Tx Output Power (dBm)	EVM (%)	Noise Figure (dBc/mHz)	Gain (db)	Applications	Modulation	CMOS Process	Advantages	Disadvantages
[59] (2006)	1.8	9.72	−2%	<35	−102 at 3.5	20	IEEE 802.15.4 WPAN	QPSK (OQPSK)	0.18 μm	Power consumption is minimized to 9.72 mW Dissipates no dc current in the mixer Improves stability	Poor sideband rejection Extremely high LO leakage (−30 dB) EVM <35% only
[58] (2007)	1.8	30.6	4.7%	8.4	–	18	Zigbee	OQPSK	0.18 μm	Linearity is improved EVM is improved to 8.4% Current consumption is reduced	Gain control range is 18 dB Amplitude mismatch in the system
[61] (2007)	1.8	16.2	−2%	<13	–	30	802.15.4 WPAN	Direct I/Q modulation	0.18 μm	Linearity is improved greatly Second harmonics are reduced	Decreases the output power Produces unwanted high-frequency signals
[62] (2012)	1.8	30.06	5%	5	−108 at 1	33	Zigbee	OOK	0.18 μm	LO leakage is minimized Tx output power is maximized	High power consumption Reduced EVM performance
[9] (2015)	1.5	183	4%	−33.6	–	86	TD-LTE	QAM	0.13 μm	Good carrier leakage suppression High gain control range of 86 dB	High PN of −120.1 dBc/Hz at 1-MHz offset High power consumption of 183 mW
[64] (2014)	1.2	10.2	0%	–	–	20	IEEE 802.15.4	–	0.13 μm	Low power consumption High linearity	Multiple harmonic signals are produced by the DAC High local oscillator leakage of 33 dBc

WPAN: wireless personal area network; OOK: on–off keying.

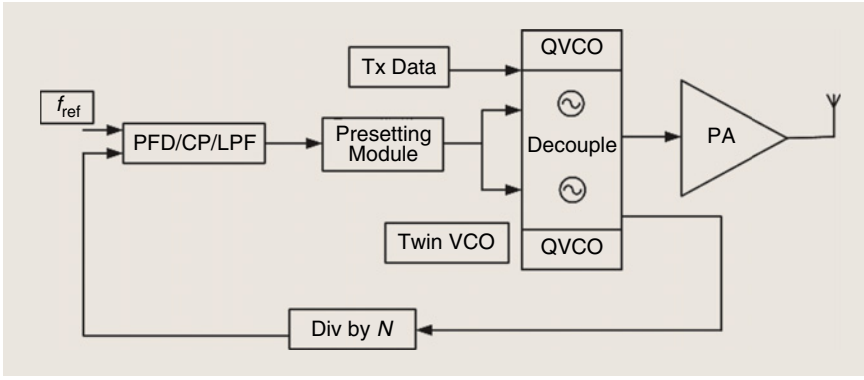

Figure 16. *A PLL-based Tx operating in transmit mode [68]. CP: channel power; PFD: phase frequency divider.*

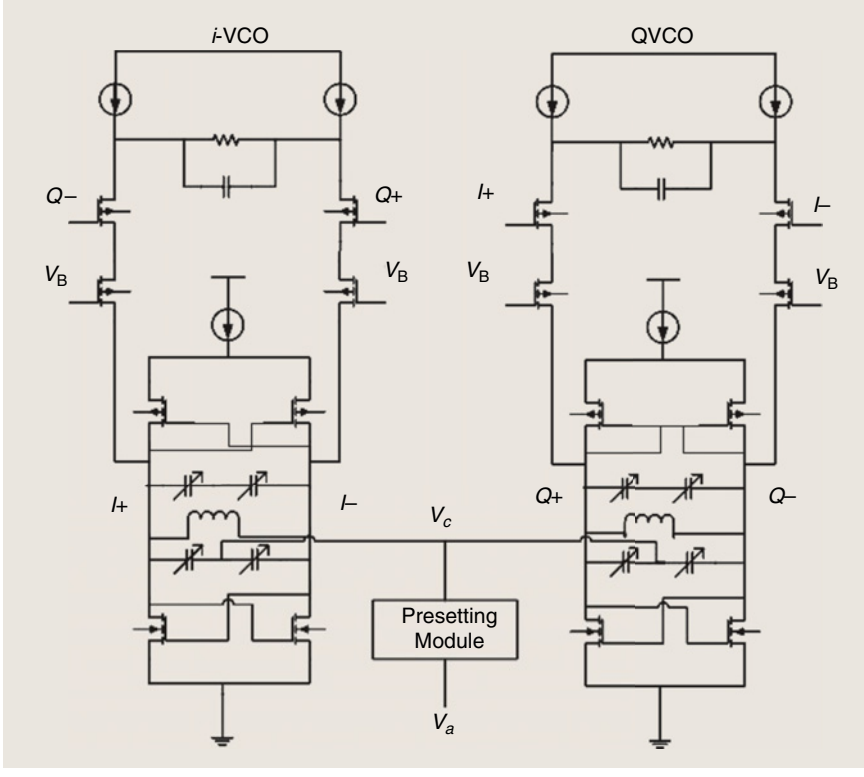

Figure 17. *The twin-VCO model proposed by Chen et al. [68]. VCO: voltage controlled oscillator.*

and VCO direct-modulation modes. The chip occupies only 1.3 mm^2 of the silicon area and obtains a maximum transmission data rate of 4 and 2 Mb/s while maintaining 0-dBm output power. Moreover, during FSK/on–off keying (OOK) modulation, the Tx dissipates 5.4- and 2.7-mA current, respectively, from a 1.8-V power supply. The resulting energy efficiency is 1.2 and 4.8 nJ/b mW, respectively, when stabilized to the transmitting power, and the improved PN is −102 dBc at 1 MHz [68]. However, high nonlinearity is experienced because of the multiple V–I conversions in the mixer stage. This Tx is one of the more suitable architectures for high-data-rate transmission with low power consumption.

Kluge et al. proposed another PLL direct-modulation-based, fully integrated 2.4-GHz Tx architecture for ZigBee applications [55]. This architecture is designed for high output power and high linearity. The PA output stage operates in saturation above the 1-dB compression point. The bias operating point is adjusted so that it can operate in class-AB mode, which helps obtain high output power. A PLL-based OQPSK direct-modulation scheme is used in this design. It delivers +3 dBm to the 100-Ω differential antenna port. The problem with this architecture is that it consumes high power of 28.26 mW [55].

Chia et al. proposed a PLL-based Tx for outdoor positioning applications, such as animal tracking. Here, the Tx operates at 868-MHz and 2.4-GHz frequencies [18], respectively. To meet the targeted Tx output of 10 dBm and increase energy efficiency, class-E amplifiers are used in this architecture. High positioning accuracy is achieved by utilizing the binary-offset-carrier technique. To enhance the positioning accuracy within 100–150 m from the object to the base station, two RF carriers are modulated by two reference frequencies. The external reference frequency of 5 MHz is used in the PLL [18]. The main advantage of this architecture is that each block of the circuit can be turned off independently by external enabling signals to conserve power during frequency settling time and sleep mode. However, this architecture suffers from nonlinearity and a lowered data transmission rate.

In [67], a small initial frequency error ΔF is utilized to reduce lock-in time. To accurately preset the target frequency during the PLL start up, the control voltage of the VCO should be biased to $V_{DD}/2$, and the loop switch should remain open. Then, the frequency of the VCO versus P[2:0] and C[5:0] for each P signal can be measured by a frequency sampler at five sampling

points. However, in [68], an LC-tank VCO that encloses a presetting module is proposed. The oscillation frequency of this VCO is derived accurately by the output signals C of the digital processor and is finely tuned through the presetting module. Kluge et al. [55] used a single LO signal in their proposed design for the RF front end. Hence, very little power consumption is needed by this design to generate and buffer the LO–Q signal. Hsieh et al. selected the carrier frequency using an external frequency-control signal [18]. Binary phase-shift keying (BPSK) modulation is implemented during the modulation stage, which is obtained by a differential 0/180°-phase shifter controlled by a corresponding subcarrier frequency at each band. No extra frequency source is required for modulation because the feedback chain of the PLL offers the subcarriers of both bands.

The performance, including the advantages and disadvantages of different PLL-based Tx architectures, is detailed in Table 5. Here, the PLL-based Tx design proposed by Chen et al. [67] achieves a higher data rate of 18 Mb/s and has less settling time than that presented in [68]. However, the design proposed by Zhang et al. [68] is more energy efficient than the architecture discussed in [67]. An optimum energy efficiency of 1.2 nJ/b mW at OOK modulation and 4.8 nJ/b mW at FSK modulation, respectively, was achieved by Zhang et al. in [68]. Kluge et al. [55] achieved 3-dBm output power from a Tx by implementing a class-AB mode PA at the expense of high power consumption. Chia et al. [18] designed a Tx capable of accurate positioning within the range of 100–150 m: however, this Tx has the drawback of nonlinearity. The designs in [67] and [69] are intended for medical and healthcare applications. The work reported in [69] presented a design with better performance in terms of EVM. Chen et al. [67] proposed an architecture that required 7-μs PLL lock-in time, contrary to the 80 μs required in [69]. Nevertheless, in [69], an architecture was proposed that implements a two-point direct-modulation scheme with a fractional-N synthesizer. This setup results in a high-output power of 9 dBm; with the help of a high-pass VCO path, the overall modulation achieves excellent EVM performance.

Subharmonic and Injection-Locked QVCO-Based Tx

Wang et al. developed a subharmonic and injection-locked (SHIL) QVCO-based Tx architecture for healthcare applications [71]. To improve linearity and design a low-power RF Tx, two design techniques were implemented. First, the multitank doublet technique was implemented in the mixer to improve linearity. This architecture consisted of a quadrature upconversion mixer, a differential to the single-ended converter (DSC), and a two-phase PA. Secondly, the multitank doublet technique was again implemented in the mixer to improve linearity, and the QVCO implemented SHIL methods to produce quadrature outputs, as presented in Figure 19. As shown in Figure 20(a), the locked transistor doublets (M5–M8) increase the transconductance while retaining low power consumption. The differential pair with an active current mirror is also implemented in the DSC structure, as shown in Figure 20(b).

Although advances in CMOS technology have improved Tx performance, the power consumption, linearity, and compactness of Txs demand further research.

High conversion gain is achieved from a two-stage, common-source PA, and the chip area is reduced to 1.4 × 0.67 mm^2 using frequency-doubling differential pairs. The benefits of the proposed SHIL QVCO architecture are minimum power consumption of 8.3 mW, low PN (–126 dBc/Hz at a 1-MHz offset), and high linearity.

Discussion

In the era of CMOS technology, the development of single-chip, low-power CMOS Txs for the 2.4-GHz band has increased significantly because of the demand of low-power, low-cost solutions for different network protocols such as ZigBee, IEEE 802.11b, and Bluetooth [70], [71]. The applications of these standards include commercial, home automation, industrial, consumer electronics, personal healthcare, and entertainment

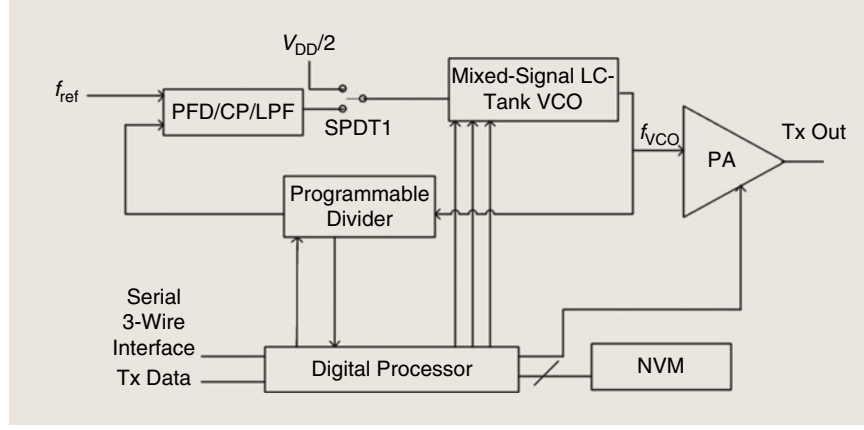

Figure 18. *The PLL-based Tx architecture proposed by Zhang et al. [69]. SPDT: single-pole doublethrow; CP: charge pump; PFD: phase frequency divider.*

TABLE 5. A performance comparison of different PLL-based Txs.

Reference Number and Year	Supply Voltage (V)	Power Consumed	Tx Output Power	Noise Figure dBc at MHz	Applications	Energy Efficiency	Modulation	CMOS Process	Advantages	Disadvantages
[68] (2013)	–	11.6 mW	0 dBm	−111 at 1	Medical	0.64 nJ/bit	FSK	0.18 μm	Energy efficient (<0.64 nJ/bit) High data rate transmission (18 Mb/s) Fast frequency-settling time Reduced chip area	High PN (−111 dBc/Hz at 1 MHz)
[69] (2011)	1.8	4.9 mW	0 dBm	−102 at 1	Zigbee, medical applications	4.8 nJ/b mW	OOK, FSK	0.18 μm	Energy efficient (1.2 and 4.8nJ/b. mW at OOK, FSK modulation) High data rate (4/2 Mb/s at OOK/FSK) Reduced PN	Creates nonlinearity High LO leakage Produces multiple harmonic signals
[56] (2006)	3	47 mW	3 dBm	–	IEEE 802.15.4	–	OQPSK	0.18 μm	Good linearity High output power of 3 dBm	Consumes high power and large chip area
[70] (2014)	1.2	34.08 mW	9 dBm	−114 at 1	Biomedical and healthcare	–	Two-points direct modulation	90 nm	Excellent EVM of 5.1% Excellent coexistence and robustness with regard to the WLAN interference	Consumes high power High PN of 11 dBc/Hz at 1 MHz

[72]–[74]. In a modern wireless communication system, the Tx is the most important functional device designed for an energy-efficient RF front end to ensure high-quality signal transmission. Although advances in CMOS technology have improved Tx performance, the power consumption, linearity, and compactness of Txs demand further research. In CMOS Tx fabrication, the important design considerations include low power consumption, high linearity, low noise figure, and satisfactory EVM performance; however, these performance parameters commonly involve a trade-off. To meet the requirements of modern RF devices, good transmission is important in downscaled CMOS technology for high-frequency applications [75], [76].

With regard to low power consumption, the CMOS process is preferred throughout the world to achieve low-power compactness and low-power operation of RF devices [77]. In this regard, an appropriate frequency modulation can help achieve a low-power, compact Tx [78], [79]. Several modulation techniques, such as GFSK, amplitude-shift keying (ASK), OOK, BPSK, QPSK, and FSK are used in Tx design to achieve low power consumption and high data-rate performance [80], [81]. Although OOK modulation presents drawbacks, e.g., sensitivity to impedance, high signal-to-noise ratio, and spectral inefficiency, OOK modulation reduces power consumption and decreases harmonics; in addition, its linear circuit architecture makes this scheme a good choice for low-power, compact Tx design [81]. Compared with the different modulations used in the body area of dynamic path-loss environments, OOK modulation is more reliable in terms of suppressing interference and harmonics [21], [60].

Several studies have been conducted to improve linearity on the signal quality of a Tx, and different modifications have been applied to different architectures. By implementing the V-NPN current-reflecting strategy, linearity execution was enhanced and carrier leakage was diminished in [60]. The Tx achieved an EVM of <13% and LO leakage of 35 dBc [60]. An LPF with various bandwidths is incorporated into this design to provide more power and area efficiency than polyphase/low-pass, reconfigurable filters. The LO leakage in [82] was removed by creating an LO-leakage calibration loop. Moreover, a dc-offset cancellation loop is created in each block of the programmable gain amplifier to suppress the dc offset in the system. The fifth-order, low-pass channel-selection filter is implemented in the Tx to provide a variable-gain feature.

A PLL, which is the heart of an FS, is a crucial and power-hungry block in a Tx design. Once operated as a component of a given system, the PLL may be subjected to interference signals that often lead to the so-called injection-pulling effect [83], [84]. Staszewski [85] and Maffezzoni showed the significance of this

effect for modern Tx and frequency-synthesis methods. Oscillatory systems are prone to injection pulling [86]; when the spectrum of the interferer is relatively close to the oscillation frequency and represents an undesired shift of this frequency, injection-pulling arises [85], [86], often having a degrading influence on the overall system performance, e.g., nonlinearity in the phase detector. The most undesirable problems occur in the VCO. The PA output in an RF Tx contains large spectral components in the vicinity of $\omega_{LO,}$ leaking through the package and the substrate to the VCO, resulting in oscillator frequency pulling [86]. To avoid injection pulling, the frequency and oscillation amplitude of the VCO design should enable a more precise estimate of perturbation transients and stability properties (as well as the oscillator output power calculation) during PLL optimization. Sancho et al. [87] proposed a method to remove injection pulling by obtaining reduced-order models for oscillator circuits around the free-running solution using harmonic-balance simulations. Razabi [86] addressed this issue by designing an oscillator model as a one-port circuit consisting of a parallel tank and a slightly nonlinear negative conductance.

The bar graph and pie chart in Figure 21 show the outcomes of Tx architectures presented in state-of-the-art works from 1992 to 2016. Tx architectures for different network protocol applications (e.g., IEEE 802.11b, 802.11g, 802.15.1, and 802.15.4) are presented, and their performances in connection with their design decisions and levels of block sharing are compared. The plotted graph shows that the dominant choice is the DCT, which accounts for 48% of the overall Tx design architectures. This Tx type presents low power consumption and easy integrability to match the receiver's path, which employs a zero-IF

A PLL, which is the heart of an FS, is a crucial and power-hungry block in a Tx design

architecture to form a transceiver. The second-most dominant design choice is the PLL-based architecture, which accounts for 28% of the overall design architecture. The superheterodyne architecture makes up only 8%, which is the lowest percentage for a specific architecture. The PLL-based Tx has been used for IEEE 802.11g mainly because of the static amplitude of its modulation signals. Most of the solutions for IEEE 802.11b, 802.15.1, and 802.15.4 (Zigbee) are simple DCT architectures with satisfactory performances covering 20, 14, and 6%, respectively. The use of a two-step-up architecture varies based on the demands of different protocols. The superheterodyne architecture is used equally for IEEE 802.11b and 802.11g and rarely for other network protocols.

With regard to Tx architectures, current studies and developments in wireless communication systems have resulted in what appear to be inconsistent methods (e.g., DCT architectures) as possible options. Although the superheterodyne architecture is used for multipurpose aspects, it needs more than one mixing step; therefore, it consumes a large amount of power and makes the Tx design highly complex [19], [30], [48]. The superheterodyne architecture should be avoided, if possible, to achieve low-cost, low-power, highly integrated multistandard solutions. The two-step-up architecture is characterized by a high analog-to-digital conversion sampling rate, which is the main reason for the high power consumption [45], [54]. It also requires

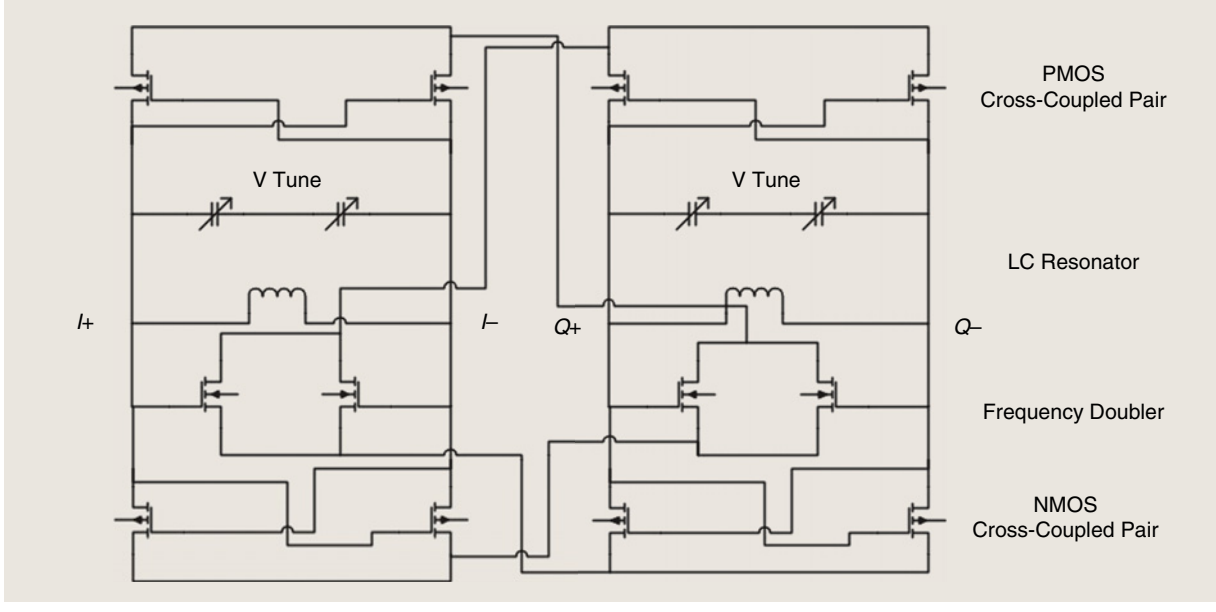

Figure 19. *A SHIL QVCO [71]. PMOS: pseudomorphic MOS; NMOS: n-channel MOS.*

Among all types of Tx architectures, the DCT has been identified as the most suitable for full system integration.

an additional image-rejection filter [43]. However, this architecture can be coordinated with the DCT architecture in the case of a large frequency contrast in the given standard.

In the two-step-up architecture, demodulation may be executed in a common IF so that the mixer can be shared [45], [88]. To meet the high reference frequency and thus obtain stability, the fractional-N PLL structure is more suitable than its integer-N counterpart [72], [88]. In the DCT architecture, the required number of functional blocks is smaller than in other architectures. The DCT architecture also does not require any image-rejection filter, unlike the superheterodyne or two-step-up architecture. It does, however, require an LPF instead of the IF BPF required in the superheterodyne architecture. All of the illustrations confirmed that the DCT is useful for wide bands with an appropriate dc-offset cancellation technique. Table 6 summarizes the design techniques, advantages, and disadvantages of each Tx architecture.

As the table indicates, the superheterodyne architecture experiences low LO leakage and less gain mismatch; consequently, low PN is generated. The drawbacks of this architecture are complex circuitry and large die size because of the extra functional block, i.e., the image-rejection filter. Although the two-step-up architecture can produce a good-quality signal, it suffers from amplitude mismatch in the LO, imaging problems, and flicker noise. While the DCT architecture is the simplest and most

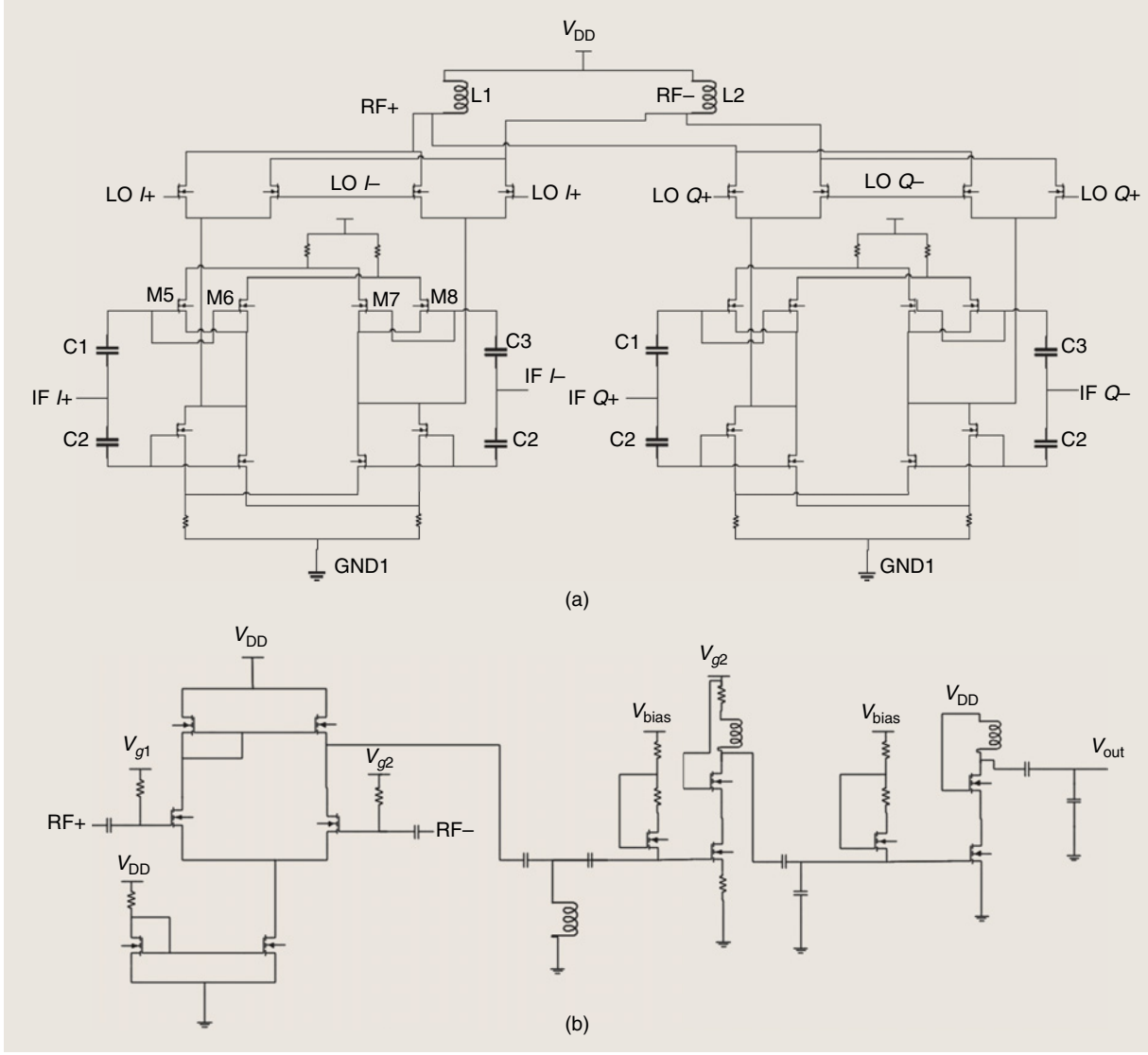

Figure 20. *(a) A quadrature upconversion mixer [71] and (b) a two-stage PA with DSC converters [71].*

popular, it exhibits higher PN and nonlinearity. Multiple V–I conversions in the upconversion mixer are the main cause of the nonlinearity in the DCT. The PLL-based architecture generates a stable VCO signal with a limited number of harmonic signals for flexible frequency synthesis. However, I/Q gain mismatch and low output power are the drawbacks of this PLL-based architecture.

Table 7 provides a summary of the results of Txs obtained from previous research by means of fully integrated topologies, including supply voltage, power consumption, CMOS process, modulation type, Tx architecture and output, chip area, noise figure, and EVM. As shown in Table 7, the Tx based on a direct-up/DCT architecture designed by Mercier et al. achieves the lowest power consumption by implementing a DAC resolution in combination with a filter order to keep PN relatively low [21]. But this architecture does not include the PLL, which consumes the most power in the design. Moreover, the lowest power-supply voltage (1 V) is supplied in this design, and OOK modulation is performed to achieve better EVM performance. The suggested architectures without the PLL block [43] and [89] consumed low powers of 7.2 and 4.5 mW, respectively. Zhang et al. [68] and Namet et al. [60] proposed architectures with a PLL block that consumes the lowest powers of 9.72 and 16.2 mW based on PLL and DCT architectures, respectively. However, Hsieh et al. [48] suggested a design based on a superheterodyne architecture, and this design consumed the highest power of 324 mW.

The method in [79] consumes a large amount of power (62 mW) because of large parasitic capacitances

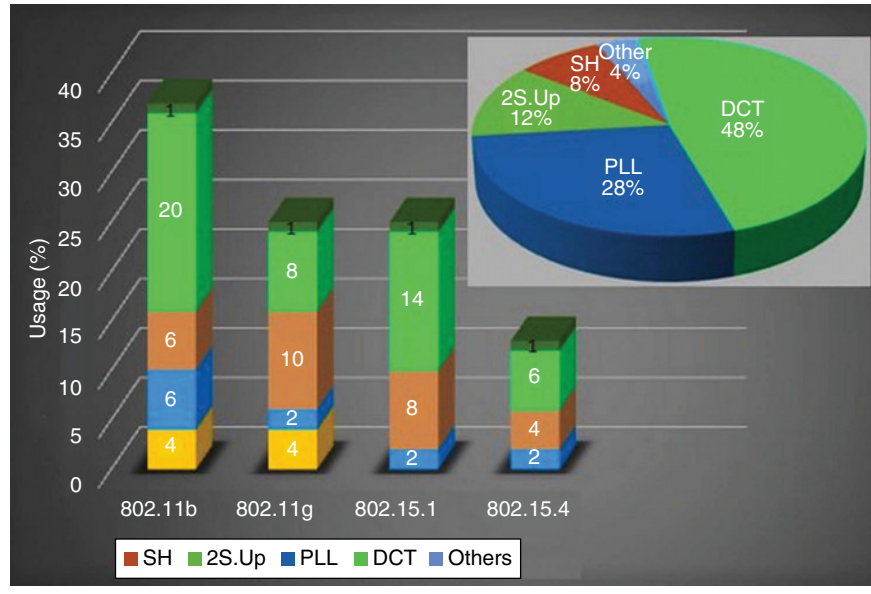

Figure 21. *The transmitter architectures employed in state-of-the-art devices. 2S.Up: two-step-up.*

TABLE 6. A performance review of recently reported CMOS Tx architectures for 2.4-GHz applications.

Tx Architectures	Design Techniques/Descriptions	Advantages	Disadvantages
Superheterodyne Tx	Only one channel is upconverted during transmission. Signal reception varies. The desired channel is surrounded by numerous unknown power in-band and out-of-band interferences.	Low LO leakage High-quality transmitted signal Low PN Flexible frequency plan	Circuit complexity High power consumption Expensive and bulky Large die size
Two-step-up Tx	Complex filters are adopted to reject the image. Low-frequency interference from the DAC and LPF can be canceled using an ac coupling.	Good ACPR Highly linear High-quality signal High output power Allows independent dc biasing for each functional block	High power consumption Unwanted sideband is produced at output Amplitude mismatch Image problem and flicker noise
DCT Tx	Techniques, such as offset VCO and LO-leakage calibration, are necessary to meet the standard required for modulation mask.	Low power consumption Minimal dc-offset noise Simplest architecture No image problem	Nonlinearity High LO leakage High PN Limited by the well-known LO pulling
PLL-based Tx	FS can be performed in PLL-based Tx by an integer-N fractional-N, and direct-digital synthesizers to obtain stable output frequency.	Energy-efficient and significant EVM performance Relaxed frequency synthesis Improved stability Reduced harmonic signal	Low output power High dc-offset noise and PN I/Q gain mismatch

TABLE 7. A performance comparison of various architectures of the 2.4-GHz transmitter.

Publication Year and Reference Number	Parameters								
	CMOS Process (μm)	Power Supply (V)	Architecture	Power Consumption (mW)	Modulation Type	Tx Output Power (dBm)	Die Size (mm^2)	Noise Figure (dBc/Hz) at Offset (MHz)	EVM (%)
2003 [46]	0.25	2.5	Dual conversion	16*	GFSK	0	1.83 × 2	—	—
2005 [96]	0.18	1.8	DCT	72	—	0	2.5 × 2[a]	—	—
2005 [19]	0.13	1.5	ADPLL	73.5	GFSK	—	0.54	<−114 at 0.5	—
2005 [49]	0.25	2.7	S/H	324	—	−23	—	−117 at 1	−3.2%
2006 [59]	0.18	1.8	DCT	9.72*	—	0	1.62	−102 at 3.5	<35%
2007 [97]	0.25	2.5	DCT	7.925*	ASK	−23.21	3.6	—	—
2007 [61]	0.18	1.8	DCT	16.2	—	−2	1.9 × 1.9	—	<13%
2009 [98]	0.18	—	Open-loop modulation	19.3	GFSK	0	—	—	—
2010 [81]	0.18	1.8	PLL	18*	OQPSK	—	~1[b]	−109 at 1	—
2010 [92]	0.18	1.5	OOK modulation	4.5*	OOK	−14	0.7 × 1.2	—	—
2011 [80]	0.18	1.8	PQN technique	62.1	Phase	−5	2.5 × 2.5	−121 at 1	−29.9%
2011 [69]	0.18	1.8	PLL	4.9 OOK 9.72 FSK	OOK/FSK	0	1.3	−102 at 1	—
2011 [44]	0.18	1.2	Direct-up conversion	7.2*	—	4.5	0.9 × 1.1	—	—
2012 [82]	32 nm	1.8	PLL	27	Delay based	25	2.6	—	−31.5%
2012 [99]	0.18	1.2	DCT	7.2*	OQPSK	1.7	—	—	—
2013 [93]	0.65	1.8	Multichannel FBAR	—	MSK GMSK	−10	0.324	−132 at 1	MSK −2.14% GMSK −5.94%
2013 [100]	0.18	1.8	Direct modulation	41.22	GFSK	0.1	0.7	−108 at 1	—
2013 [83]	0.18	1.5	Open-loop modulation	9.15**	FSK	>−60	0.1	−111.8 at 0.5	—
2014 [64]	0.13	1.2	DCT	10.2*	—	0	1.76 × 1.26	—	<30%
2014 [21]	0.18	1.0	Direct-up conversion	78 pw*	OOK FSK	>−29	2.4 × 2.4	−105 at 1	—
2014 [70]	90 nm	1.2	PLL	34.08	Direct modulation	9	—	−114 at 1	5.1%
2015 [94]	65 nm	1.2	FBAR	10.44*	BPSK QPSK	0	2	—	BPSK −5.11% QPSK −6%
2016 [18]	150 nm	1.8	PLL	50.4	BOC	10	0.67	—	—

[a]: including pad; [b]: without pad; *: power consumption without the PLL block; and **: power consumption including the VCO and frequency-division module of the PLL.
BOC: binary offset carrier; FBAR: film bulk acoustic resonator; ASK: amplitude-shift keying; GMSK: Gaussian minimum-shift keying; MSK: minimum-shift keying; PQN: phase-quantization noise.

at the gates of the current mirror. Additionally, the Tx chip area is 2.5 × 2.5 mm^2, which is larger than that of other Tx chips [80], [81]. However, improvement has been achieved on its phase-quantization noise, which is reduced to 49 dB when transmitting a 20-Mb/s GFSK signal by applying a phase-quantization, noise-cancellation-path technique.

Ravi et al. designed a Tx that achieved the highest output power of 25 dBm with a significant EVM performance of 31% [81]. Paidimarri et al. proposed another Tx architecture that attained the best EVM performance: −2.14% for minimum-shift keying modulation and −5.94% for Gaussian minimum-shift keying modulation at the expense of a high PN of −132 dBc/Hz at a 1-MHz offset [90]. The lowest noise figure of −102 at a 1-MHz offset was achieved by Zhang et al. [68] with reduced die size (1.3 mm^2 only).

An average performance in linearity, low power consumption, and good output power was achieved by Kopta et al. [91]. Instead of the classical PLL-based method, the architecture in [92] utilized a film bulk-acoustic-resonator oscillator to produce the high-frequency reference signal. This setup provided several advantages, such as a much shorter start-up time compared to that of classical PLL-based architectures [92]. Moreover, no additional delay related to the settling time of the PLL is observed.

A comparison of Tables 6 and 7 suggests that the key advantage of the DCT architecture is its low power consumption while maintaining the performance of other parameters under the standard requirement. For low-power and highly linear applications, this architecture is considered the best among the mentioned architectures. Among all types of Tx architectures, the DCT has been identified as the most suitable for full system integration. Consequently, research in this discipline is incredibly active with regard to the improvement of RF devices functioning in high-frequency ranges, such as 2.4 GHz, with optimum power.

Conclusions

A detailed review of advances observed in CMOS Txs with different topologies for 2.4-GHz ISM band applications was conducted, focused on adequate design architecture, design concerns and considerations, and performance analyses. Several techniques have been implemented by different researchers to obtain improved performance of 2.4-GHz RF Txs in CMOS technology. Designing a highly linear, low-power, and compact Tx remains difficult for many designers because of CMOS downscaling factors, such as PN, leakage power consumption, and other parasitic effects. The performances of various design architectures, including their limitations and advantages, were compared. Several researchers have worked to maximize Tx output power, and several others have worked to reduce leakage current and power consumption and so obtain ultralow power. A few studies improved linearity and ACPR. Comparisons show that the DCT architecture is highly suitable for designing a 2.4-GHz RF compact Tx and can address the demand for low-power, low-cost solutions for modern wireless communication systems. The procedures of Tx design and the associated discussions presented in this article are expected to aid researchers in designing RF Txs and contribute to realizing small, low-cost wireless communication terminals at the 2.4-GHz ISM band.

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2018 Student Design Competition Winners IMS

Wireless Microwave Energy Harvesting

A Flexible Virtual Battery

Ahmed Abdelraheem, Michael Sinanis, Shahzad Hameedi, Mahmoud Abdelfattah, and Dimitrios Peroulis

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Continuous advancements in the domains of biomedical sensors, Internet of Things (IoT) devices, in vivo sensors, and other similar technologies have created a great need to miniaturize portable and end-user devices, especially their powering circuitry. Nearly all devices and sensors require a powering mechanism to obtain, process, and/or transmit information. For example, [1] discusses a flexible gastric battery and a wireless power link that can replace traditional bulky batteries and reduce the size of the wireless capsule. Low-power circuit solutions are of paramount importance for wearable and implantable devices to reduce battery size and improve user comfort [2]. Harvesting the available unused microwave energy from, e.g., Wi-Fi and cellular signals seems a promising solution for replacing a conventional battery with a *virtual battery*. This term has been used in [3] to describe RF-to-dc converters that are able to power small, portable

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RF applications for a reasonably long time in the absence of a direct illuminating RF field.

The IEEE Microwave Theory and Techniques Society (MTT-S) Student Design Competition for wireless microwave energy harvesting, held during the 2018 MTT-S International Microwave Symposium, this past June, required the competing teams to construct, measure, and demonstrate a wearable wrist wireless energy harvester (WEH) at 2.45 GHz, capable of powering a small electronic device. The designed WEH was expected to harvest power densities ranging 1–10 $\mu W/cm^2$. In this article, we summarize our design flow and experimental results for this application.

Antenna Design

While designing a rectenna for ambient microwave power harvesting (AMPH), we needed to consider three key factors. First, in AMPH, very limited RF power is available, often below -35 dBm. Although such power levels are considered quite strong for typical communication applications, they are relatively weak for generating dc voltages. We quantitatively discuss this in the following section. Second, the rectifier's efficiency primarily depends on the available RF power level at the rectifier's input terminal, so we needed to carefully consider this in the design flow. Third, the antenna needs to capture as much power as possible from the very limited ambient RF power. Consequently, the antenna design typically precedes the rectifier design. We start by discussing the antenna type and substrate in the next two sections.

Substrate Selection

The competition rules required the rectennas to be suitable for wearable applications. This narrowed down the potential substrates to those that are very thin and flexible. Commercially available flexible substrates typically range from 25 to 150 μm.

To understand the limitations imposed by this thickness range, we considered the thickness requirements for both the antenna and the rectifier. The first limitation relates to bandwidth: a typical microstrip patch antenna's bandwidth is proportional to its substrate thickness [4]. As shown in the next section, wide bandwidth is a requirement for the initial antenna design.

The second limitation relates to radiation efficiency; a microstrip-patch antenna's efficiency degrades rapidly for thicknesses below 0.01 λ_0 [4]. This is a desirable feature when selecting the rectifier substrate; therefore, a thick substrate is preferred for the antenna, while a thin one is needed for the rectifier. To fulfill both requirements, we used a multiple-layer design, explained in the next section.

Similar considerations apply for the substrate dielectric constant—i.e., at low permittivity, higher radiation efficiency and wider bandwidth are obtained [4]. Moreover,

The anticipated input power levels affected our selection of the rectifier topology, optimal diode, and optimal load.

the selected substrate has to survive all of the fabrication process steps, including the soldering of the components.

Based on these considerations and practical fabrication process constraints, we selected the Pyralux-AP 8555 R substrate with the following characteristics: thickness = 125 μm; copper clad = 18 μm; dielectric constant = 3.4; and loss tangent = 0.002.

Antenna Design Procedure

Because the rectenna was being designed for wearable applications, it had to be conformal and nonobstructive. This entails withstanding bending conditions. Bending may affect the antenna's center frequency and bandwidth; therefore, if the antenna is very narrow band, even slight changes may detune it. We also wanted our antenna to have a full ground plane to isolate it from the human body–loading effects and absorptive losses. Adding such a ground plane, though, could restrict the antenna bandwidth, as previously discussed.

First, we focused on an ultrawide-band slot antenna design [5]. This is the antenna represented by the top two layers depicted in Figure 1, where the elliptical slot is the main contributor to the radiation. The U-shaped tuning stub is meant to achieve coupling between the feed line and the elliptical slot. The size of the elliptical slot controls the lower edge of the bandwidth. This was selected such that the bandwidth starts at a frequency slightly below 2.45 GHz. To add a full ground plane while keeping the elliptical slot, we inserted a 2-mm–thick foam layer between the ground plane and the antenna. Thanks to this foam layer, the antenna had sufficient thickness beneath the elliptical slot; at the same time, the rectifier (which is outside the elliptical slot) was implemented on the thin substrate. Moreover, after inserting the foam layer, the rectenna was still sufficiently flexible for wearable applications.

To accurately model the foam layer in the full-wave simulation, we extracted its dielectric constant and loss tangent by measuring a conventional microstrip transmission line on the foam substrate. These values were approximately 1.1 and 0.03, respectively.

After adding the full ground plane to the back side of the foam layer, we performed some geometry adjustment to center the antenna frequency to 2.45 GHz. Furthermore, the bandwidth became narrow, as expected. Despite these drawbacks, this ground plane helps isolate the antenna from the human body, as illustrated by the plotted three-dimensional radiation pattern in Figure 2(a). This isolation is not perfect, and the saline-water-bottle cylinder in

In [9], it was shown that, for low input powers, minimizing the loss due to diodes and filtering capacitors is key for high power conversion efficiency.

Figure 2(a) does result in some detuning. Nevertheless, one feature of the proposed antenna is that its resonant frequency depends on the substrate length denoted as L in Figure 1. This can be easily inferred from the current distribution in the slotted ground plane and is illustrated in Figure 2(c), in which the simulated S_{11} of the proposed antenna is shown for different values of L: 31.5, 30.5, 29.5, and 28.5 mm. This adjustment is readily achieved without the need to refabricate by trimming the antenna length.

In Figure 2(c), the proposed antenna is mounted on a saline-water bottle, which simulates human-body-loading effects. In Figure 2(d), we show the measured antenna matching performances for four different cases. Case 1 is the fully planar (no bending) and unloaded (no saline water) version. As expected, case 1 (red line) exhibits the widest bandwidth. Case 2 (black line) is the bent but still unloaded antenna with a bending radius of 35 mm. Case 3 (dotted blue curve) is the bent antenna mounted on a saline-water bottle with a bending radius of 35 mm (same as case 2) to simulate the human-body effect. We can observe the frequency shift that resulted from the saline-water effect. This shift was compensated for in case 4 (solid blue line) by trimming the length L of the antenna. For cases 1, 2, 3, and 4, the measured input impedances at 2.45 GHz are 48.2 + j3.2, 47 − j7.6, 16.7 + j7.9, and 28.7 + j14.4 Ω, respectively. The values of S_{11} associated with these impedances are −29 dB, −21 dB, −6 dB, and −10 dB, respectively.

Bending and loading it with a bottle of saline water detuned the antenna, resulting in a mismatch represented by a 6-dB return loss. After we trimmed the antenna, the matching resulted in a 10-dB return loss. The length mentioned in the caption of Figure 1 is the length of both the standalone antenna and the rectenna before trimming. We prefer to show this length because the trimmed length used to tune the antenna is different from that used to tune the rectenna: the standalone antenna is tuned to exactly 50 Ω of the attached connector, whereas the integrated antenna is tuned to the imperfect input impedance of the integrated rectifier.

We fabricated the antenna/rectenna using a conventional photolithography process. A Pyralux substrate was first coated with Dry Film Negative Photoresist and then exposed to ultraviolet light to transfer the pattern, after which it was developed in a sodium bicarbonate solution for 5 min. We etched the copper using CE-100 copper etchant with full immersion and agitation. Finally, substrates were cleaned with acetone and isopropanol alcohol.

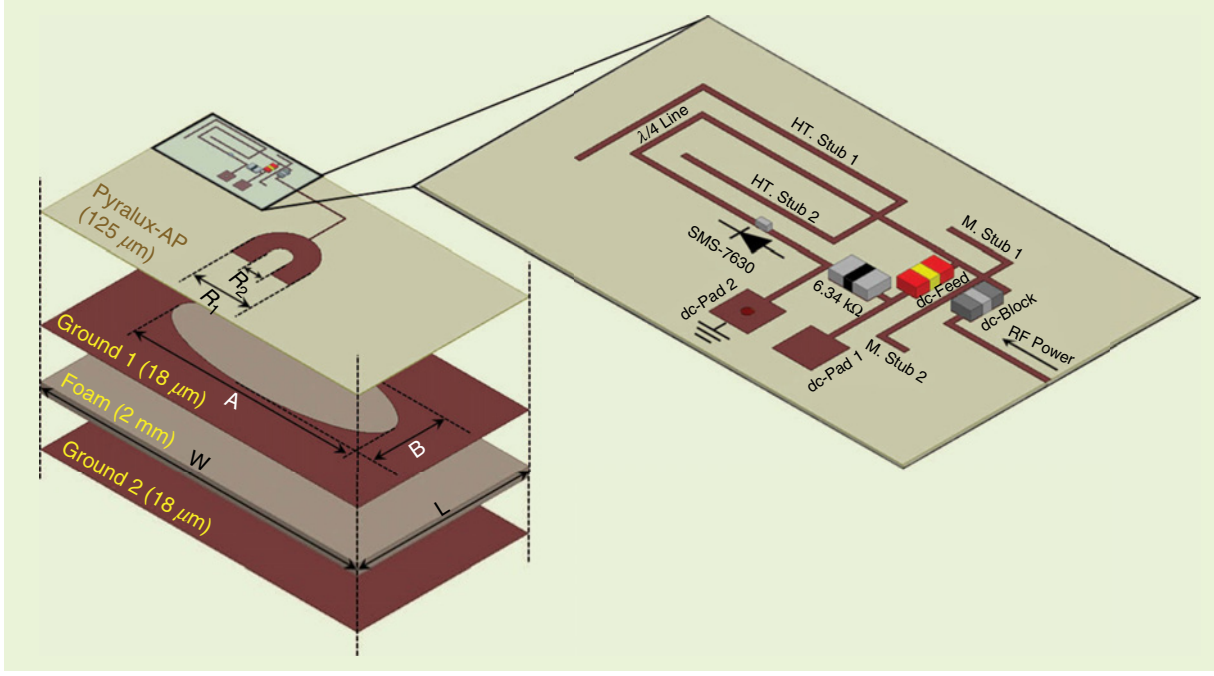

Figure 1. *A three-dimensional representation of the different layers of the proposed rectenna, including a close-up of the rectifier layout with all necessary components. Layer names and thicknesses are printed on each layer. $W = 59.5$ mm, $L = 29.5$ mm, $A = 22$ mm, $B = 9$ mm, $R1 = 7$ mm, and $R2 = 4$ mm. W: substrate width; L: substrate length; A: elliptical slot major axis; B: elliptical slot minor axis; Pyralux-AP: a family of Pyralux substrate; HT: harmonic termination; M: matching; SMS-7630: diode part number.*

Rectification: The Core of Power Conversion

Because rectification is the core of RF-to-dc power conversion, the rectifier design is of critical importance to the overall performance of the rectenna. The anticipated input power levels affected our selection of the rectifier topology, optimal diode, and optimal load.

The competition rules limited the incident power density to 1–10 μW/cm^2. Considering a 2-dBi gain (e.g., a standard monopole antenna), we estimated the input power as -25 to -15 dBm. However, because practical ambient microwave power harvesting can be as low as -35 dBm [6], we presented our rectifier performance down to -45 dBm.

The next selection in the design process was the nonlinear element of rectification. At such low levels of input power, the nonlinear element is zero-biased. For such applications, we needed a low-barrier diode rather than an on/off, high-barrier one. This limited the range of input powers in which the rectifier could operate efficiently. The primary reason was that the video resistance (nonlinear junction resistance plus diode series resistance) decreases rapidly as the input power increases. This, in turn, makes designing the matching network more difficult. To give the reader a sense of the numbers, the video resistance can vary from a few kiloohms to a few hundred ohms in the off region of a low-barrier Schottky diode. Moreover, at high video resistance (which corresponds to the lower limit of the RF power and thus is called the *zero-bias resistance*, or *ZBR*), the dc power delivered to the load is quite small.

Class F power amplifiers achieve high efficiency by minimizing the overlap between voltage and current waveforms within the transistor, and the same concept can be exploited in rectifiers to achieve high PCE.

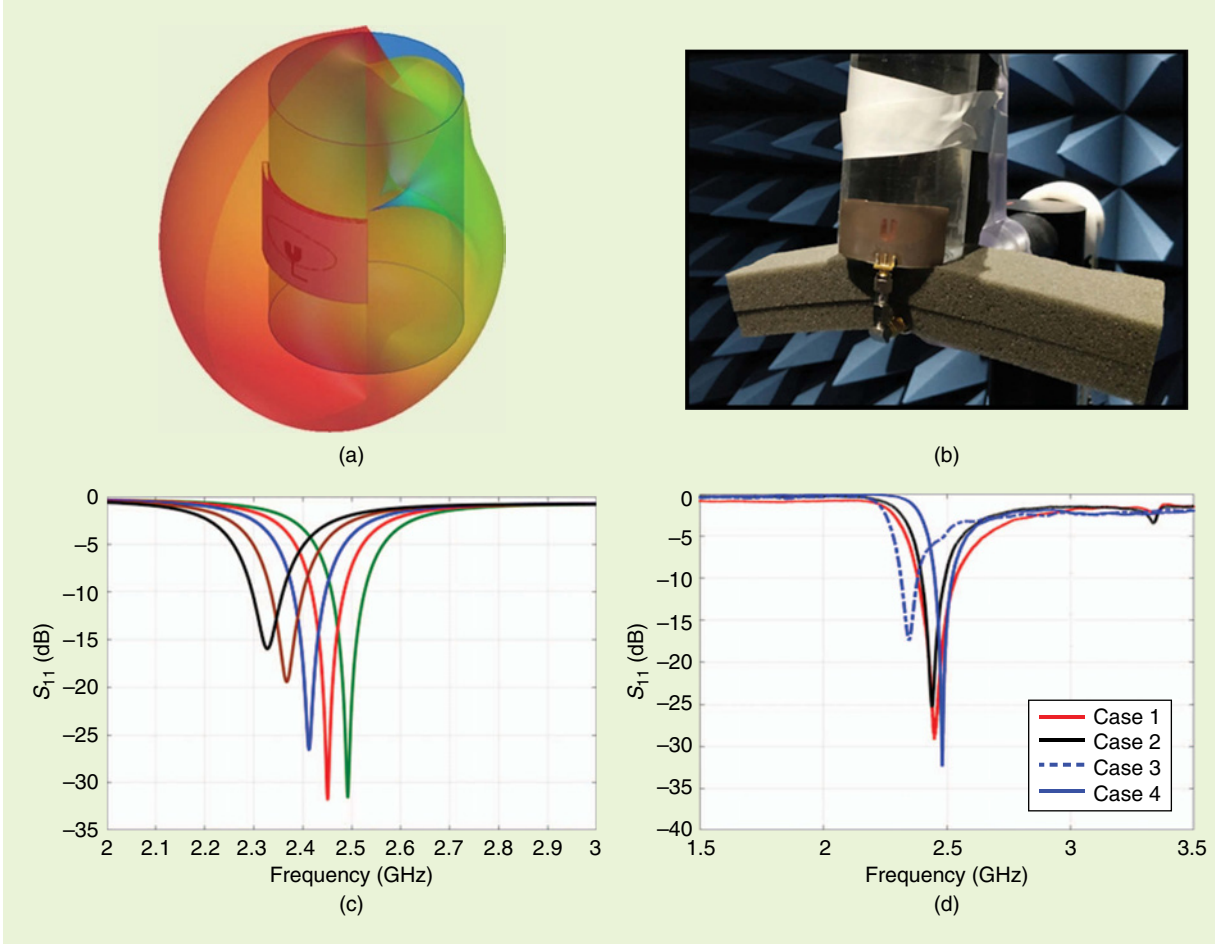

Figure 2. *The proposed antenna results. (a) The simulated three-dimensional radiation pattern of the antenna mounted on a saline-water bottle with cylinder radius of 35 mm. (b) A photo of the antenna mounted on a saline-water bottle inside the anechoic chamber. (c) The simulated S_{11} of the antenna for different values of length L (Figure 1). (d) The measured S_{11} values for four different cases (described in the text) that include bending and saline-water-bottle loading effects.*

In [7], a thorough investigation revealed that magnetic tunnel junctions technology is an excellent candidate because of its significantly lower ZBR compared with the available low-barrier Schottky diodes. In addition, this investigation also included a comparison between commercially available diodes that may be good candidates for AMPH. The study described in [8] also compared the performance of commercially available diodes. Based on these comparisons, we selected the SMS7630-061 (0201 surface-mount technology package) diode for this work. This diode features a small built-in potential (0.34 V), a small junction capacitance (0.14 pF), relatively small series resistance (20 Ω), reverse saturation current (4 μA), and a high cutoff frequency that reaches 26 GHz.

After selecting the nonlinear element of rectification, we determined the rectifier topology. In [9], it was shown that, for low input powers, minimizing the loss due to diodes and filtering capacitors is key for high power conversion efficiency (PCE). This entails using the minimum number of such components, so here we used a topology with only one diode. Class F power amplifiers achieve high efficiency by minimizing the overlap between voltage and current waveforms within the transistor, and the same concept can be exploited in rectifiers to achieve high PCE [10]. We achieved this waveform shaping in the design by terminating the second and third harmonics.

The layout depicted in Figure 1 shows $\lambda/8$ and $\lambda/12$ open stubs placed $\lambda/4$ away from the shunt diode. These are designated as "HT. Stub#2" and "HT. Stub#1" in Figure 1 and are meant to terminate the second and third harmonics, respectively. As mentioned in [6], the low-power optimum load approximately equals the junction resistance of the zero-biased diode. Consequently, a 5-kΩ load was selected as an initial load. Further optimization resulted in 6.34-kΩ load value.

For the antenna-captured RF power to be properly transferred to the rectifier, the rectifier's input impedance had to be matched to the 50-Ω input antenna

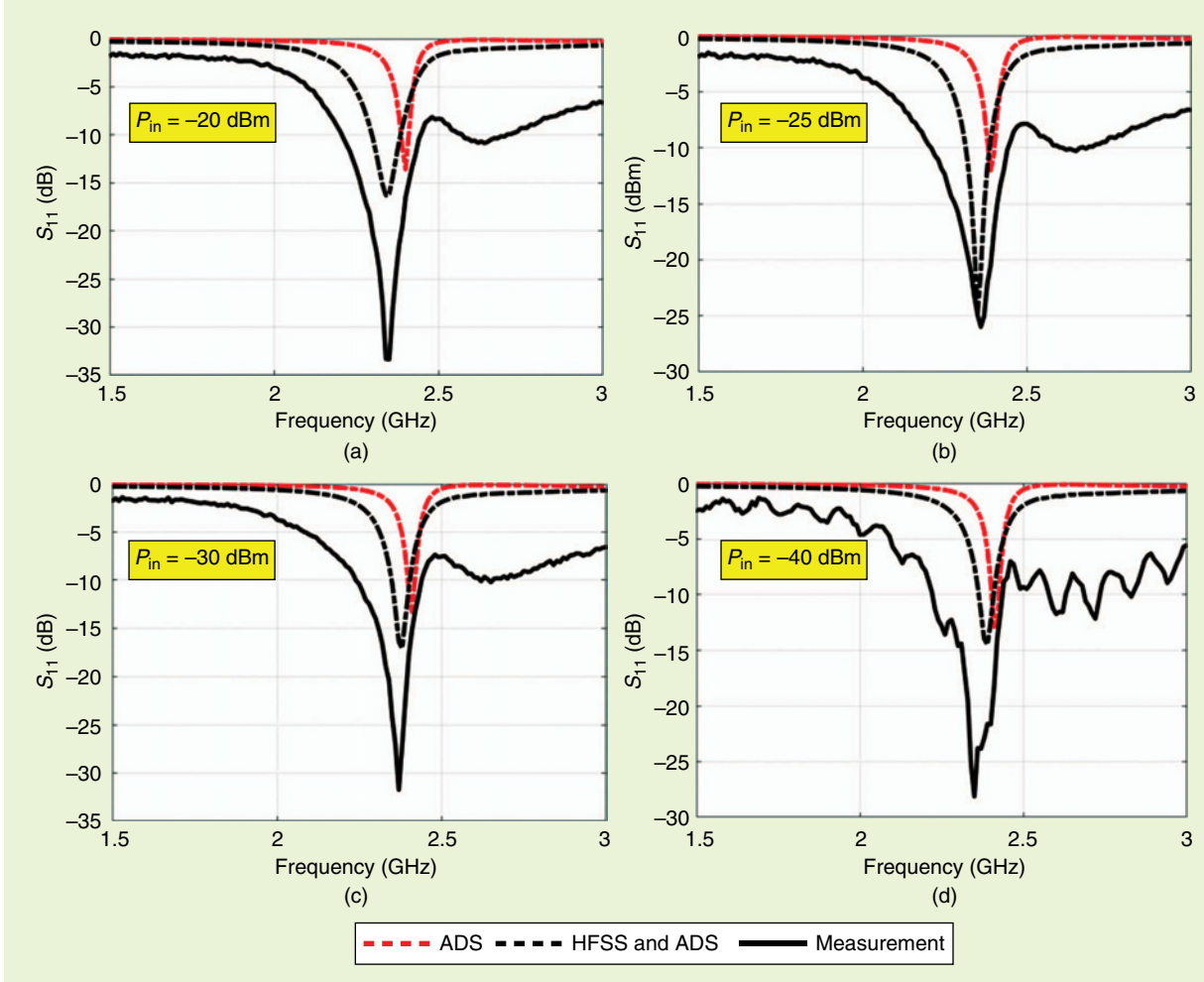

Figure 3. *The simulated and measured S_{11} of the proposed rectifier for different levels of RF input power: (a) –20 dBm, (b) –25 dBm, (c) –30 dBm, and (d) –40 dBm.*

impedance. We used a double stub-matching network, designated as M. "Stub#1" and "M. Stub#2" in Figure 1. As mentioned, because of the low barrier of the diode, the input impedance of the rectifier varies with varying input RF power. As a result, the matching network should account for this variability.

To ensure this, we optimized the matching network at 2.45 GHz and over RF power levels that ranged from -40 dBm to -15 dBm. We modeled the diode, using the Advanced Design System (ADS) simulation package, as a symbolically defined device (SDD) by inserting the diode equations in this SDD model to account for the diode's nonlinearity. This is essential at lower RF levels, because the entire rectification process happens in the nonlinear region. Moreover, to accurately simulate the transmission lines and their coupling effects, a full-wave simulation of the rectifier layout was performed in the ANSYS high-frequency structure simulator (HFSS), including the components' footprints. The results of this simulation were then linked with the SDD model of the diode in ADS.

To illustrate the difference between full-wave and transmission-line model simulations, we present both simulated and measured results in Figure 3. The figure shows that HFSS full-wave simulation results show better agreement with the measurements. The discrepancy can be attributed to the imperfect modeling of the package parasitics in the simulation.

We measured the fabricated rectifier for different RF power levels from -40 dBm to -20 dBm (Figure 3). As can be seen, good matching was preserved over a wide range of input powers. Before integrating this rectifier with the proposed antenna, we directly connected the rectifier to a signal generator to investigate the output dc voltage. The simulated and measured output dc-voltage versus RF-power results were in good agreement, up to approximately -15 dBm (Figure 4). We attribute the discrepancy to the difference between the values of the package's parasitic capacitance and inductance used in the simulation (data sheet values) and the real values that contributed to the measurement.

An optimum distance between the transmitting and receiving antennas had to be defined first so we could measure the widest range of RF input powers at the rectenna end.

Integration (Rectenna Results)

Integrating the designed antenna and rectifier into a rectenna was the final step in the design process. This integration resulted in slight changes in the responses of the stand-alone components. These changes were mainly due to the connector-loading effects and are highlighted below. To simulate the human-body effect in the competition, we mounted all of the designs on a plastic bottle of saline water that acted as a human phantom.

A test setup that fulfills this constraint was reproduced in our laboratory inside the Purdue University anechoic chamber. We used a signal generator to provide different levels of RF power in the wireless local

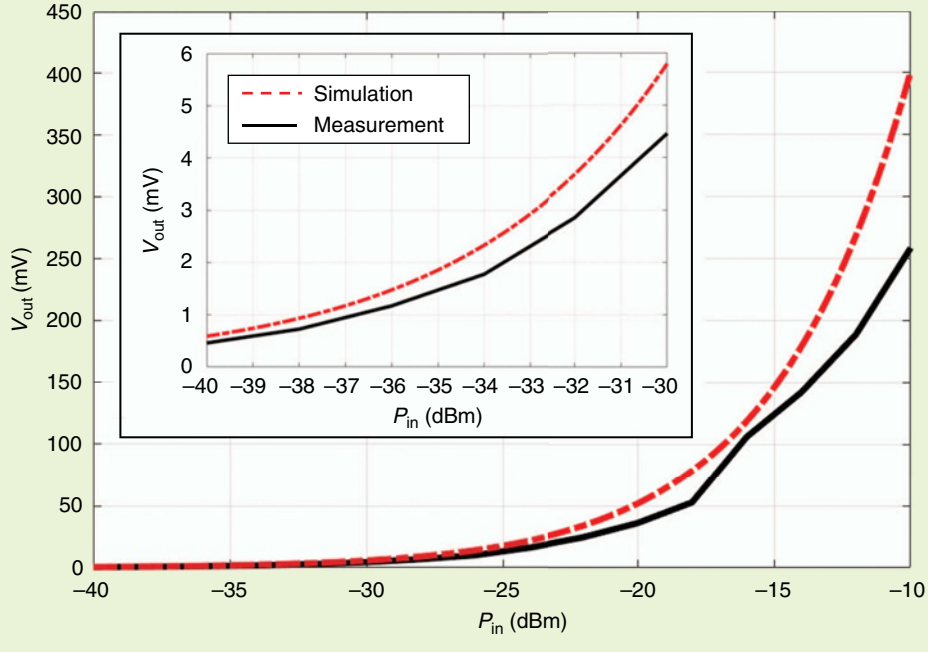

Figure 4. *The measured output dc voltage (V_{out}) of the proposed rectifier versus input RF power in decibel-milliwatts.*

area network (WLAN) frequency band and a standard monopole antenna with 2-dBi gain for transmitting. The signal generator provided power levels up to 19 dBm.

An optimum distance between the transmitting and receiving antennas had to be defined first so we could measure the widest range of RF input powers at the rectenna end. The setup used to measure the total path loss due to this distance is illustrated in Figure 5(a). In this case, the optimum distance was the minimum far-field distance for the larger of the two antennas. The standard monopole antenna's largest dimension was greater than its counterpart in the proposed antenna; therefore, we used it to calculate the far-field distance employing the well-known rule of thumb

$$R_{\text{farfield}} \geq \frac{2D^2}{\lambda}, \tag{1}$$

where D is the largest antenna dimension and λ is the wavelength at the center frequency. A distance of 12 cm is defined to be the optimum distance. Given this selection and based on the measured gain of the bent-loaded antenna (2.1 dBi), RF power levels from -50 dBm to approximately -5 dBm can be provided at the rectenna's end.

The setup for measuring efficiency is illustrated in Figure 5(b). To study the bending and human-body loading effects, we measured the rectenna in the following cases: flat unloaded, flat loaded, bent unloaded, and bent loaded. The receiving antenna gain was different for all four cases, so the exact input RF power level to the rectifier was different for all four cases. To properly account for this, we measured the rectenna's dc voltage and efficiency versus the incident power density for each case separately. These results are reported in Figures 6(a) and (b).

We can observe from the figure that bending results in a slight degradation in the measured dc voltage and efficiency. This can be attributed to the degradation of the

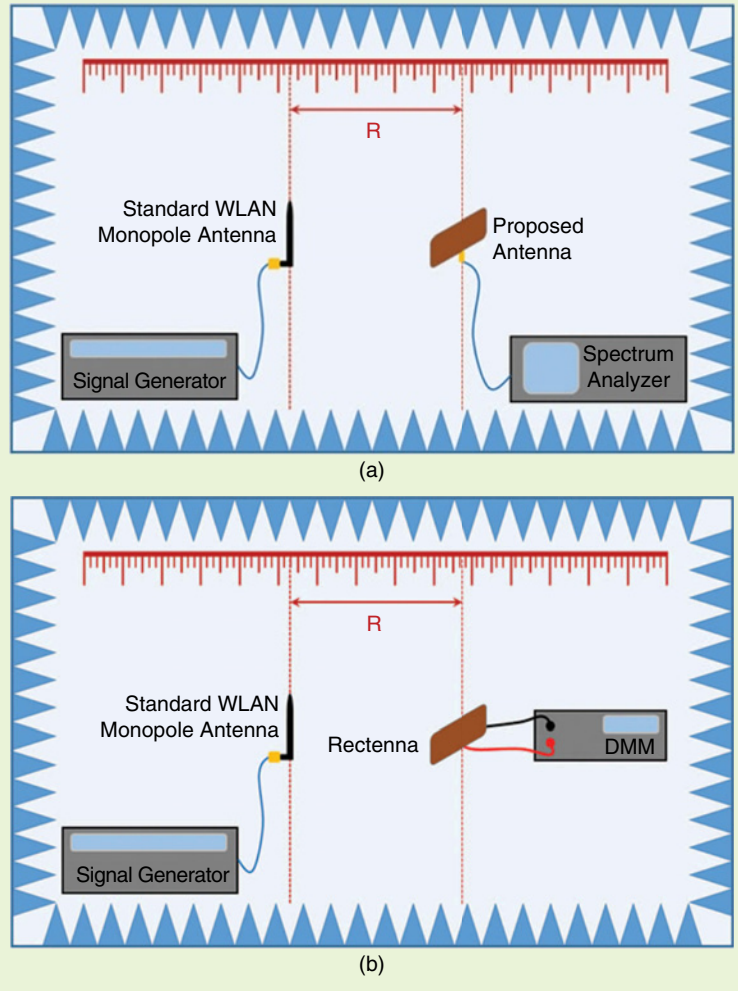

Figure 5. *(a) The measurement setup to determine the optimum distance, R. (b) The measurement setup of the proposed rectenna efficiency inside the anechoic chamber. DMM: digital multimeter.*

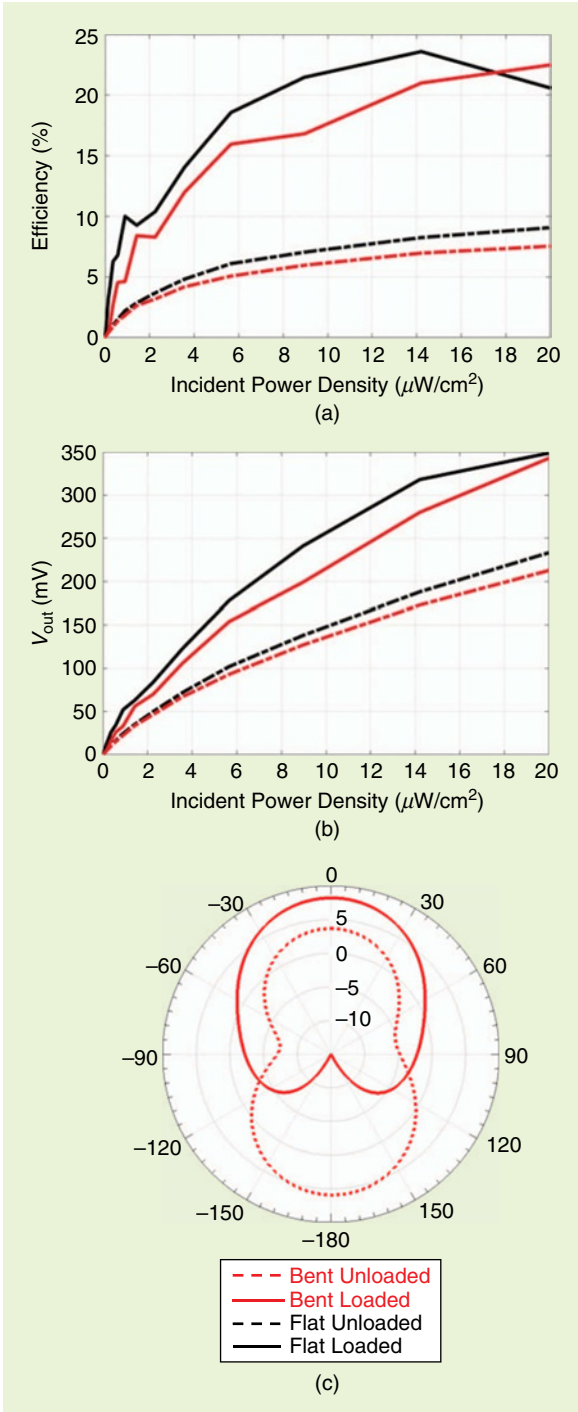

Figure 6. *The final rectenna's (a) measured efficiency versus incident power density and (b) measured dc voltage versus incident power density. (c) The simulated directivity of the integrated antenna before and after loading with the human phantom. V_{out}: output dc voltage.*

antenna performance in terms of gain and bandwidth. The bandwidth degradation effect can be inferred from the antenna results depicted in Figure 2(d). Also, we can observe that loading the rectenna with a phantom simulating the human-body effect increases the dc voltage and efficiency. This is because the phantom enhances the directivity in the direction of maximum illumination, as can be seen from the simulated directivity of the loaded and unloaded bent antenna in Figure 6(c). The maximum directivity increased from 3.7 to 8 dB after loading the antenna. We compensated for the loading effect on the integrated antenna impedance (and, hence, the mismatch) by trimming the rectenna until maximum efficiency w obtained for the bent-loaded rectenna. Figure 6(a) shows that the efficiency was 5%–20% in the range of 1–10 μW/cm^2.

Conclusions

We presented the design process of a wearable wireless energy harvester. We adopted a multilayer configuration to meet the contradictory substrate requirements for the antenna and the rectifier. To account for the practical operating conditions, we first measured the antenna under bending conditions and human-body-loading effects (using a saline-water bottle). Results confirmed that the antenna stays tuned under all of these conditions. We also measured the final rectenna under the same conditions. The efficiency of the final rectenna in the most practical case (bent loaded) ranged 5–23% over the incident power densities required by the competition, 1–10 μW/cm^2.

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2018 Student Design Competition Winners IMS

Carrier Aggregation BAW Quadplexer Module

Multiplying Channel Capacity

Yuchen Cao, Emil Jesman Sunde, and Kenle Chen

The explosive growth of mobile Internet-based applications and ecosystems has been driving insatiable demands for data transmission speed. From third generation to fourth generation, the typical data rate of cellular networks has been significantly enhanced from a megabits-per-second to almost a gigabits-per-second level [1]. According to Shannon's communication theory, an increase of frequency bandwidth plays the key role in expanding channel capacity. However, the highly scattered allocation of long-term evolution (LTE) bands does not support contiguous expansion of bandwidth and acts as the major barrier to further channel capacity enhancement. Therefore, the LTE Advanced standard proposed the concept of carrier aggregation (CA) for the first time, as illustrated in Figure 1(a) [2]. This enables concurrent operation of multiple spectral resources such that the channel bandwidth can be effectively multiplied without increasing the signal-to-noise ratio across the entire channel [3].

The LTE standard specifies that each component carrier (CC) of the communication signal is limited to 20 MHz of bandwidth. Aggregation of up to five CCs leads to a maximum

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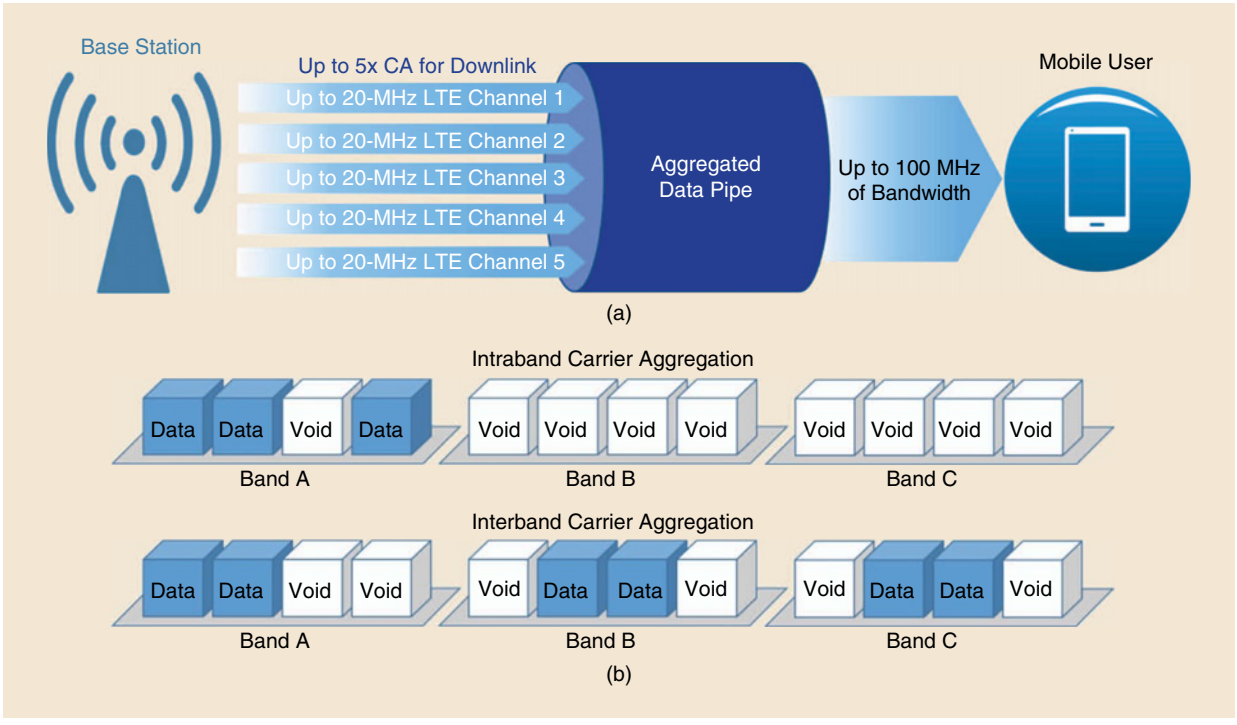

Figure 1. *The CA illustration of the (a) CA air interface and (b) different CA modes.*

100 MHz of total signal bandwidth, as depicted in Figure 1(a). This leads to a fivefold increase of channel capacity and data speed. There are two types of CA, intraband and interband [4], [5], as shown in Figure 1(b). Intraband CA does not require a change of front-end hardware, because the CA signal is still within its frequency coverage. Because more spectral resources can be used across different bands than within a single allocated band, interband CA is a more general and popular case, and it also requires hardware upgrades. The interband CA in base stations can be enabled using multiple antennas and advanced digital signal processing [6]. However, these two luxuries are not available in mobile handsets because they are limited by space, computational capacity of the digital back end, and the battery's power capacity. As a result, the interband CA in handsets is commonly performed at the RF front end (RFFE) without a more sophisticated, ultrapowerful digital backend.

Cellular Handset RF Front-End Architecture for CA

There are more than 30 different communication bands for the latest LTE band allocation, spanning 700 MHz–2.7 GHz. In the wireless industry, this range is commonly divided into three RF bands based on optimized feasibility of RF design, including a low band at 700–960 MHz, a midband at 1.6–2.3 GHz, and a high band at 2.5–2.7 GHz. The RFFE system is required to support all 30-plus bands for global roaming phones. Figure 2 shows a typical architecture of RFFE on mobile handset platforms, which consists of three parts: the multiband, multimode power amplifier, the filter bank, and the antenna switch. The CA is mainly supported by advanced filter technologies, known as the *multiplexer*, which enables concurrent operation of different RF bands [7], [8].

Emerging Filter Technologies in Mobile Handset Platforms

RF filters are essential components in the radio front-end systems of emerging mobile handset devices (Figure 2) for spectral isolation, interference blocking, radio coexistence, harmonic rejection, and so on, each of which requires a dedicated filter (e.g., time-domain duplexing) or a duplexer (e.g., frequency-domain duplexing). Because of limited space on the phone board and extremely congested spectral allocation of bands, the filters need to offer a very high quality factor (Q factor) for high isolation and low insertion loss while maintaining an ultracompact form factor. As for such stringent requirements, surface-acoustic-wave (SAW) and bulk-acoustic-wave (BAW) technologies offer satisfactory solutions for filter implementation on handsets.

SAW and BAW devices take advantage of acoustic-wave propagation, vibrating at a resonant frequency related to their dimensions and mechanical properties. In this sense, the resonator behaves like an acoustic cavity, trapping the wave in the medium. A SAW is an elastic wave that travels along the surface of a crystal substrate in the lateral direction, whereas a BAW is an elastic wave traveling inside solid-layered material in the vertical direction [9]. BAW resonators have

demonstrated a higher Q factor than their SAW counterparts. The state of the art for BAW resonators is Q factors of 2,000–3,500 below 3 GHz. In contrast, the best SAW resonators achieve Q factor values of only up to 2,000 [10]. Therefore, BAW devices are more suitable for higher-frequency operation (e.g., midband and high band) and performance-oriented, high-end phones. Film-bulk-acoustic-resonator technology can be considered a special BAW technology that is able to further improve the Q factor, e.g., beyond 4,000. However, its complicated geometry results in yield issues and high costs for massive manufacturing.

Quadplexer for Dual-Channel CA

Frequency-domain duplexing dominates LTE communications. To separate the transmit (Tx) and receive (Rx) paths in the frequency domain, two BAW filters are combined in parallel, forming a three-port device named the *duplexer*, which allows concurrent transmission (uplink) and reception (downlink) using a shared antenna. To support dual-channel CA, two duplexers need to be combined to enable concurrent operation of two different bands through a shared antenna. This leads to an integrated quadplexer module, which is a five-port device.

Figure 3 shows the detailed operation of the front-end configuration, enabling CA of bands 3 and 7. It consists of four paths, including two Rx paths and two Tx paths. The RF signal transmission between the antennas (port 1) and the Tx/Rx port (ports 2–5) must cover four frequency bands. The band 3 Tx (port 2) has a frequency range of 1,710–1,785 MHz, the band 3 Rx (port 3) has a frequency range of 1,805–1,885 MHz, the band 7 Tx (port 4) has a frequency range of 2,500–2,570 MHz, and the band 7 Rx (port 5) has a frequency range of 2,620–2,690 MHz. Each filter in the quadplexer is expected to be well matched for the passband frequencies and open for the cross-band frequencies.

The quadplexer module was designed and implemented for the IEEE Microwave Theory and Techniques Society 2018 International Microwave Symposium Student Design Competition (IMS2018 SDC) "CA BAW Quadplexer Module." The design and implementation are based on TQQ1003 and TQQ1007 BAW duplexers manufactured by Qorvo, Inc. Our design target for the competition was focused on the in-band insertion loss and return loss of all ports and on the isolation between

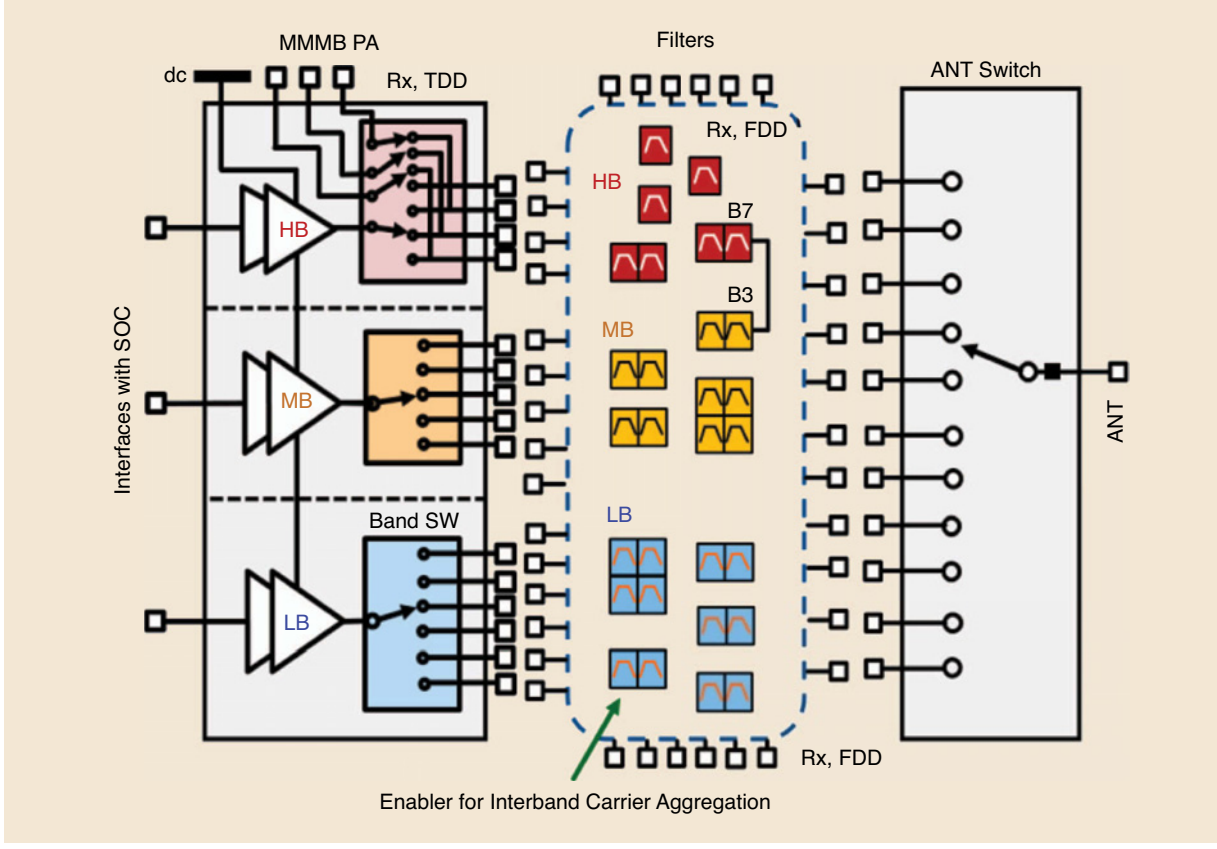

Figure 2. *The mobile-handset RF front-end architecture enabling carrier aggregation at the filter/multiplexer bank. Rx: receive path; FDD: frequency-division duplex; TDD: time-division duplex; HB: high bandwidth; MB: midbandwidth; LB: low bandwidth; SOC: system-on-chip.*

in-band Tx/Rx ports and cross-band ports. The entire circuit was implemented on Rogers RO4003C substrate, and the RF design was performed using Keysight's Advanced Design System (ADS). This IMS2018 SDC specified a maximum insertion loss of fewer than 6 dB, a return loss greater than 10 dB, and an isolation larger than 30 dB as minimum requirements. Our design achieved the best possible performance.

Design of the Quadplexer Module

We based our design on four main considerations, as follows.

Insertion-Loss Optimization with Phase Shifting

The quadplexer was realized by physically connecting the antenna nodes of the band 3 and band 7 duplexers. Ideally, one duplexer needed to present an open circuit

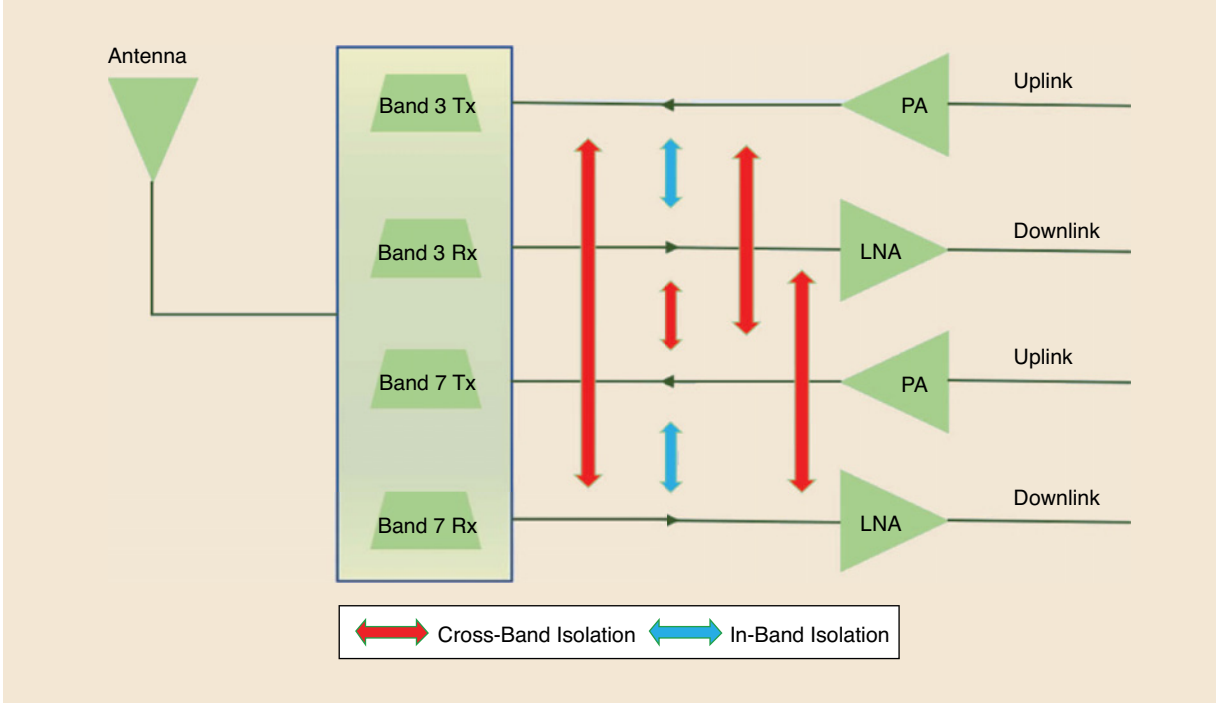

Figure 3. *The quadplexer topology for band3 and band7 carrier aggregation. LNA: low-noise amplifier; PA: power amplifier; B: band.*

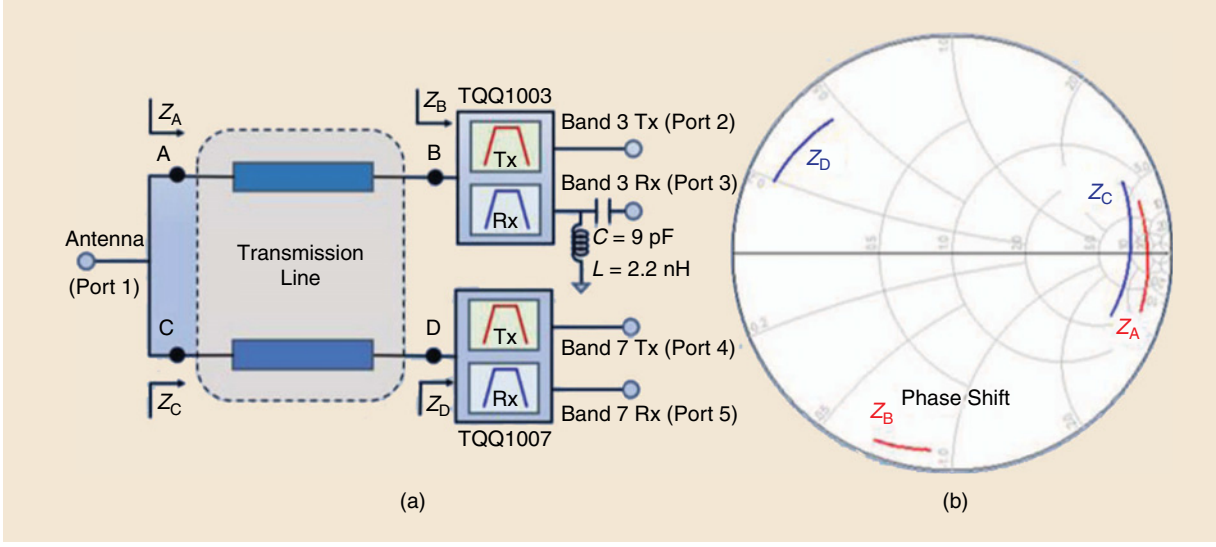

Figure 4. *The quadplexer design with insertion loss optimized by phase shifting: (a) the circuit schematic and (b) an illustration of the phase shifting from simulated results.*

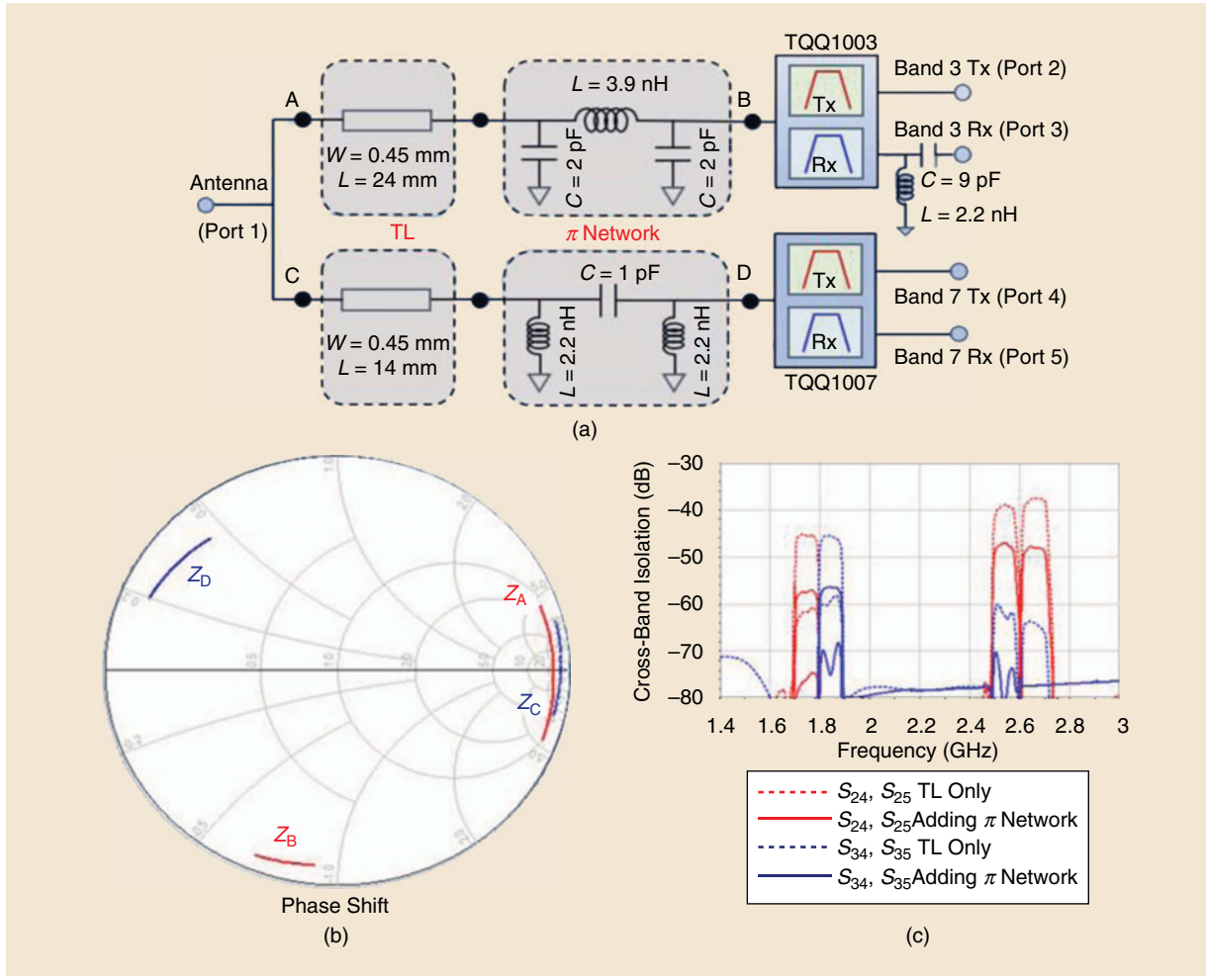

Figure 5. *The quadplexer design with π networks for enhanced cross isolation: (a) the circuit schematic, (b) illustrations of the phase-shifting results, and (c) the cross-band isolation improvement comparison.*

at the passband frequency of the other duplexer so that the passband transmission did not suffer from distortion and degradation. Specifically, the band-3 duplexer needed to provide an open circuit (high impedance) at the band-7 frequency, and vice versa. Because the standalone duplexers were not naturally equipped with these characteristics (see Figure 4), phase shifters were needed at the antenna nodes. The phase shifters were easily implemented using transmission lines (TLs) with dedicated electrical lengths, as indicated in Figure 4. The 50-Ω TLs not only transformed the two duplexers' cross-band antenna-node impedances to open circuits; they also maintained the initial in-band impedances, which were 50 Ω as well. At the combining node, the open-circuit impedance was achieved at the passband of the other path, as shown in the Smith chart of Figure 4.

Enhancement of Cross-Band Isolation with π Networks

Although the TL-based phase shifter was able to provide the desired impedance transformation, it did not offer any filtering functions. As a result, the cross isolation depended solely on the BAW filters' rejection at the cross-band frequencies. To achieve better performance in terms of cross-band isolation, we partially replaced the TL phase shifters with π-networks (Figure 5). These filter networks offer not only the same phase-shifting functions but also additional filtering at cross-band frequencies. We introduced a low-pass filter network into the band-3 path and a high-pass filter network into the band-7 path. The values of the inductors and capacitors of the π network could be tuned to change its bandwidth and the rejection level at the cross-band frequency.

Given the general compromise between the filter's stopband rejection and passband insertion loss, we made certain trade-offs in the values of the two π networks to achieve optimized overall performance. Together with the TL-based phase shifters, the cross-band impedances of two duplexers were tuned to nearly open circuit. Comparing Figure 4(b) with Figure 5(b) shows that the π networks enhanced the overall rejection closer to the cross-band frequencies,

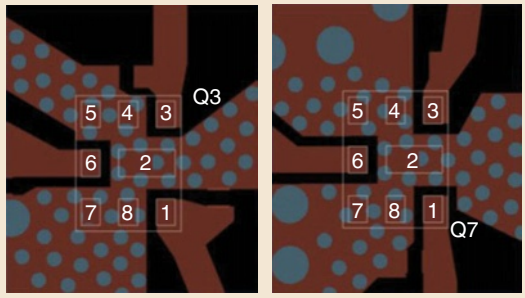

Figure 6. *Two duplexer ground shielding layouts: (a) the TQQ1003 duplexer ground shielding and (b) the TQQ1007 duplexer ground shielding. Q3: quality factor for band 3; Q7: quality factor for band 7.*

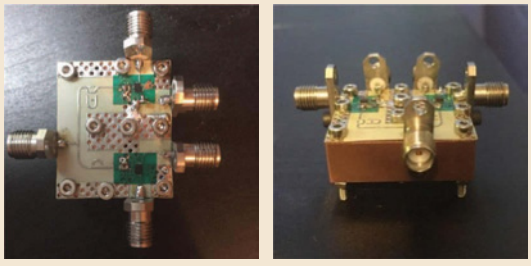

Figure 7. *The fabricated demonstration circuit board: the (a) top view and (b) side view.*

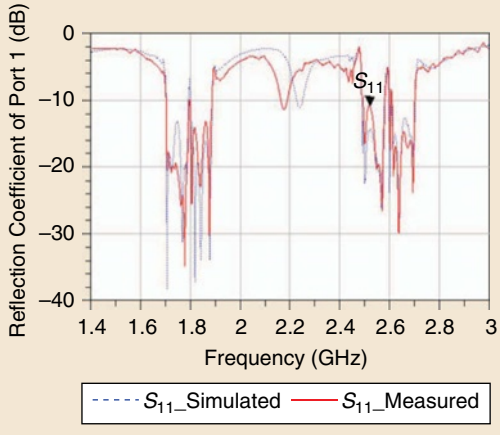

Figure 8. *The reflection coefficients at the antenna port.*

leading to better cross-band isolation by 10–15 dB, as shown in Figure 5(c).

In-Band Isolation Design

The in-band isolation of the duplexer was determined by 1) the BAW duplexer's intrinsic isolation, 2) electromagnetic coupling between lead structures of Tx/Rx/antenna ports, and 3) interaction between the printed circuit board (PCB)

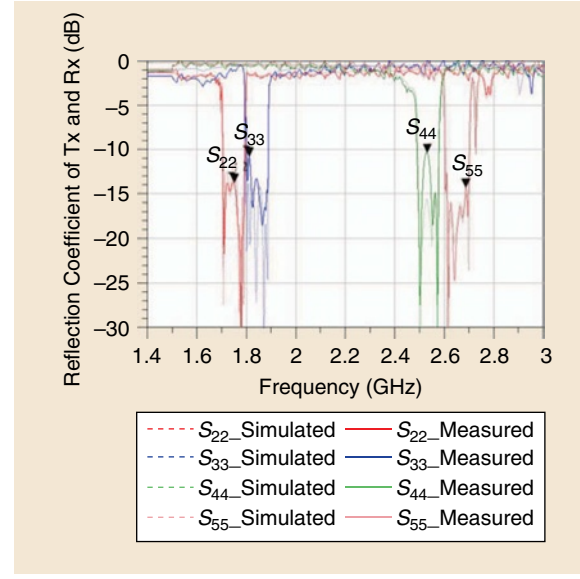

Figure 9. *The reflection coefficients at the Tx and Rx ports.*

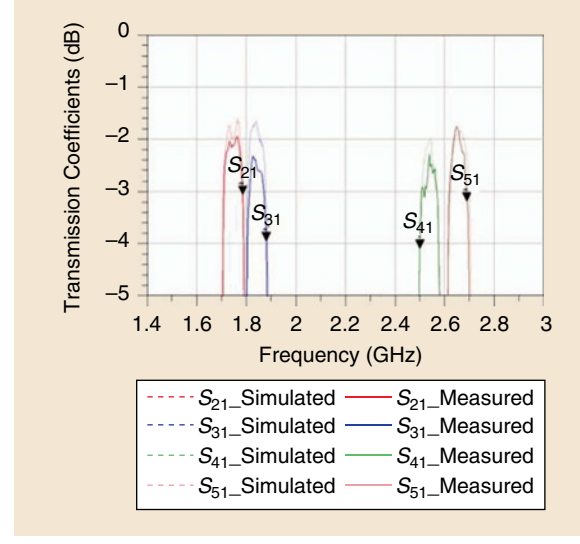

Figure 10. *The transmission coefficients between antenna port and Tx/Rx ports.*

and the duplexer die. To minimize the coupling between ports, we inserted a shielding structure, formed by grounding via holes, between the Tx, Rx, and antenna lead traces. Figure 6 shows the PCB layout of the duplexer, illustrating that a number of via holes were placed as ground shielding, which isolated different ports. The coupling strength also depended on the height of the via, which effectively represented the inductance shunt to ground.

To minimize this ground inductance, we reduced the height using an 8-mil thickness of PCB. However, electromagnetic (EM) simulation with the black-box duplexer model did not accurately represent the actual isolation because the board–die interaction was not captured. Multiple variants of the PCB layout had to be generated

to experimentally optimize the isolation, and multiple rounds of development iterations were necessary, but such costs was prohibitive for an academic group. Therefore, the isolation design was performed based on EM modeling of the PCB (using Keysight ADS FEM simulator) and co-simulation with black-box duplexer models.

Inductor and Capacitor Circuit Matching at Band-3 Rx Port

Based on experimental measurement, we found that the Rx port matching of band 3 (port 3) was not as ideal as the simulation results. The deembedded results showed that the intrinsic port impedance was capacitive with a real part larger than $50\,\Omega$, and a high-pass L-section matching network is added to the Rx port side of the TQQ1003 to improve the return and transmission losses, as shown in Figure 4.

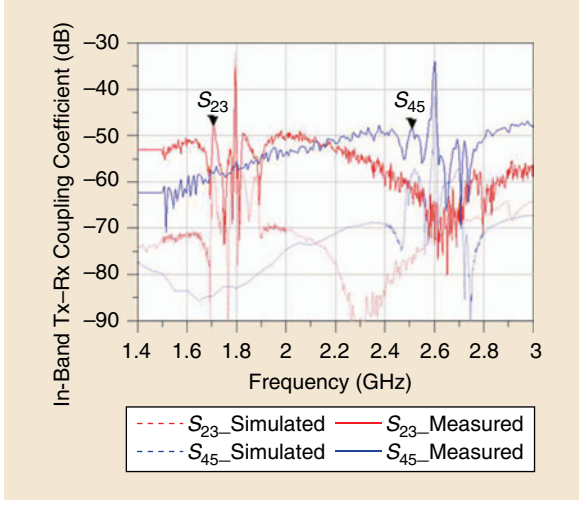

Figure 11. *The in-band Tx/Rx isolation performance in band 3 and band 7.*

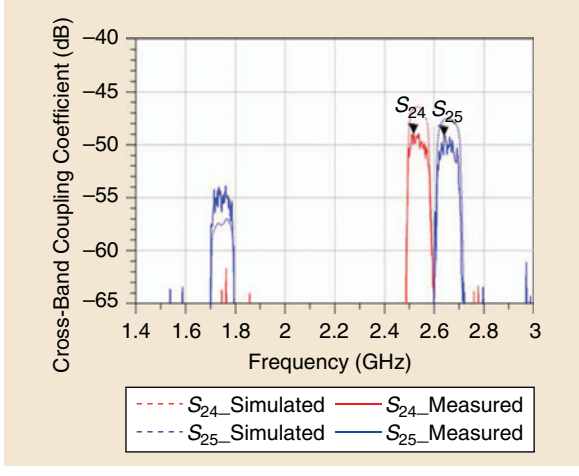

Figure 12. *The cross-band isolation performance between the Tx port of band 3 and the Tx/Rx ports of band 7. P2,4: ports 2 and 4; P2,5: ports 2 and 5.*

Device Fabrication

The quadplexer module based on the previous design considerations was fabricated on a RO4003C substrate, with a relative dielectric constant of 3.55, substrate thickness of 8 mils, and loss tangent of 0.0027. The populated board was then attached to a copper substrate to strengthen the handling of the entire device. The fabricated module is shown in Figure 7 with both the top view and side view. The board size was $25 \times 30\ \text{cm}^2$, as specified in the competition rules.

Measurement Results

The performance was measured using an Agilent N5230C vector network analyzer from Keysight Technologies. The measured reflection coefficient of the antenna port is shown in Figure 8 and was in good agreement with simulation results. The antenna port presented a low reflection coefficient (fewer than -10.8 dB) across the entire frequency range of band 3 and band 7. Figure 9 shows the measured reflection coefficients of all of the Tx and Rx ports of the quadplexer. The measured output reflection coefficients were fewer than -10.3 dB in both band 3 and band 7. Figures 8 and 9 show that all of the ports were well matched for dual-band CA.

Figure 10 shows the measured and simulated transmission coefficients of the implemented quadplexer. The measured transmission coefficients of the signal paths through the antenna port to the Tx/Rx ports were greater than -4.1 dB (i.e., <4.1 dB of insertion loss) within the respective passbands. The worst-point in-band of each path is indicated by a marker in Figure 10 and typically occurred at the band edge. Because the band-3 Rx (S_{31} in blue) and band-7 Tx (S_{41} in green) are close to the passband edge of the π networks, the insertion loss of these two paths was slightly degraded as a trade-off for cross-band isolation.

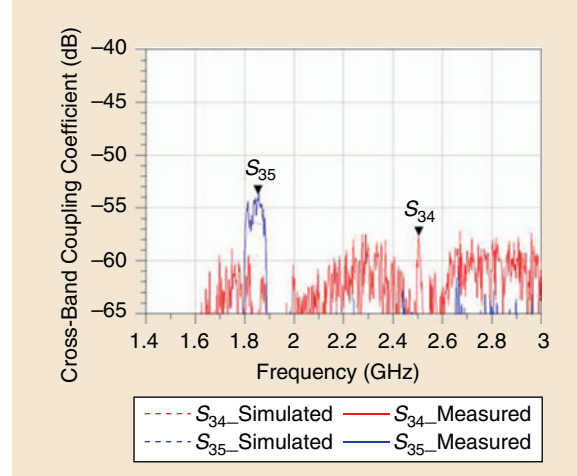

Figure 13. *Cross-band isolation performance between Rx port of band 3 and the Tx/Rx ports of band 7.*

TABLE 1. A performance comparison with winning design of 2017 [11].

Design (Size)	Antenna Port Return Loss, dB	Rx/Tx Port Return Loss, dB	Insertion Loss, dB	In-Band Isolation, dB	Cross-Band Isolation, dB
2017 winner (30 × 30 cm^2)	10.5–30	10.3–30	1.8–3.7	39.4–61	38.6–57
2018 winner (25 × 30 cm^2)	10.8–35	10.3–30	1.8–4.1	47.9–65	49–70

The measured and simulated in-band isolation performances are shown in Figure 11. The in-band coupling coefficients from measurement are fewer than -47.9 dB for band 3 (red) and band 7 (blue), leading to greater than 47.9 dB of isolation between the Tx and Rx paths. This is attributed to the ground shielding placed underneath the duplexer die that isolated the leakage between different ports. Figure 11 shows that the simulation results indicated better isolation compared to the measurement, with approximately 10 dB of difference in-band. This is possibly due to fact that the simulation based on the black-box duplexer model was inaccurate for in-band isolation, because the interaction between the PCB and duplexer die was not captured, as discussed in the previous section.

Figures 12 and 13 show the measured cross-band coupling coefficients between band 3 and band 7, including the band-3 Tx to the band-7 Tx (S_{24} in red in Figure 12), the band-3 Tx to the band-7 Rx (S_{25} in blue in Figure 12), the band-3 Rx to the band-7 Tx (S_{34} in red in Figure 13), and the band-3 Rx to the band-7 Rx (S_{35} in blue in Figure 13). The cross-band isolations from the measurement were greater than 49 dB, and the measured results were in good agreement with simulation. From the system perspective, Tx/Rx cross isolation at the Rx band is the most important parameter, because it determines the desensitization of the Rx when downlink CA is performed. In this design, the isolation between the band-3 Rx and the band-7 Tx is particularly favorable, i.e., greater than 60 dB within the the band-3 Rx band, offering good CA performance at the system level. Table 1 compares our results with the results of last year's winning design. Our design greatly improved the in-band and cross-band isolations, with return and insertion losses slightly compromised to optimize the overall performance.

In summary, the achieved performance we have described indicates that the transmission coefficients are greater than -4.1 dB, the reflection coefficients of all of the ports are fewer than -10.8 dB, and the coupling coefficients between each port are fewer than -47.9 dB. Therefore, all of the measured results meet the competition requirements and have been greatly improved on this basis.

Conclusions

This article describes a BAW-based quadplexer module for LTE-Advanced CA applications. Two BAW duplexers (TQQ1003 and TQQ1007) manufactured by competition facilitator Qorvo, Inc., were used in this design, and a compact module of $25 \times 30\ cm^2$ is demonstrated. To achieve the best possible performance, two LC-circuit–based π networks and two TL-based phase shifters were designed together with BAW duplexers. The dedicated phase-shifting design ensured the efficient combination of two duplexers without a mutual pulling effect, leading to the maximum transmission of four paths. Furthermore, the π networks offer additional filtering capability that enhances the cross-band isolation. Overall, the developed quadplexer module presents favorable performance for CA.

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2018 Student Design Competition Winners IMS

Backscatter Radio

Backscatter Modulation for Wearable Devices

Ricardo Correia, Daniel Belo, Felisberto Pereira, Marina Jordão, and Nuno Borges Carvalho

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The use of wearable devices is increasing as a growing number of applications is introduced. The major limitation of these intelligent and multifunctional devices is the battery-charge capacity, which restricts the applications' scope.

Most wearable devices require frequent charging, an annoyance for many, but especially for those inclined to forget to recharge their devices. Meanwhile, the need for frequent recharging makes the devices less

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attractive for those who like them particularly because they can be operated discreetly.

Multiple recent technologies have enabled the rapid spread of battery-free wearable devices, such as those that harvest kinetic energy from walking or running [1]; those powered by solar panels [2], ambient heat, or temperature changes [3]; and those that harvest RF energy [4], [5]. Another important technology that can be considered for wearable devices is backscatter communications, which enable the benefits of Bluetooth or Wi-Fi technologies but without the need to consume the power that Bluetooth and Wi-Fi require. In backscatter communications, the tag reflects a radio signal transmitted by the reader and, by presenting different load values to the antenna, controls its own reflection coefficient, thereby modulating the reflection [6].

The load modulator is usually a switching transistor that normally alternates between two different impedances. By switching the antenna impedance between those two values, the tag can modulate the RF signal in a binary fashion and scatter it back to the reader. This type of communication requires none of the active components commonly found in traditional wireless transceivers, which makes it ideal for very-low-power implementations. Each sensor is implemented with a backscatter communication module. By simply switching the impedance connected to the antenna port, the tag can communicate with the reader. The modulation schemes used most often are amplitude-shift keying and phase-shift keying (PSK) [7], [8], although other modulators have been reported [9], [10].

In health applications, researchers have made smart contact lenses for monitoring diabetes, sensing glucose, and measuring eye pressure [11]–[13]. Some of these systems include eyeglasses that are wirelessly powered and communicate to a circuit worn by a patient. Another application that uses wearable gadgets is the Google Glass system [14], which can assist in such cognitive tasks as face and speech recognition. The main drawback of these applications is the communication distance. In some cases, that distance is not more than a few centimeters.

The future of the Internet of Things will rely on smart objects with electronics containing recyclable, flexible, and biodegradable materials. A summary of possible future microwave circuits for applications in smart objects was recently published in [15].

The work presented in this article is based on the Student Design Competition (SDC) focused on backscatter radio that was organized for the 2018 IEEE Microwave Theory and Techniques Society (MTT-S) International Microwave Symposium (IMS 2018) and sponsored by MTT Technical Committee 24 (RF Identification). The design presented in this article won first prize at the competition.

Objectives and Metrics

According to the backscatter radio SDC organizers, the main objective of this competition was to design, fabricate, and test a backscatter modulator consisting of an antenna and a 1-MHz binary backscatter modulator operating at a carrier frequency of 915 MHz. The validation setup used in the competition is presented in Figure 1.

The performance of the device under test (DUT) was evaluated as a tradeoff between several design geometries: the backscattered modulation power and the power consumption for two transmitting power scenarios ($P_{TX1} = 25$ dBm and $P_{TX2} = 30$ dBm equivalent isotropic radiated power). The figure of merit (FOM) used for the evaluation is given by

$$\text{FOM} = \frac{P_{RX1}(\text{nW}) + P_{RX2}(\text{nW})}{P_{C1}(\text{uW}) + P_{C2}(\text{uW})} \times \frac{100}{D1\,(\text{cm}) + D2\,(\text{cm})} \times \frac{100}{\text{weight}\,(\text{g})}, \quad (1)$$

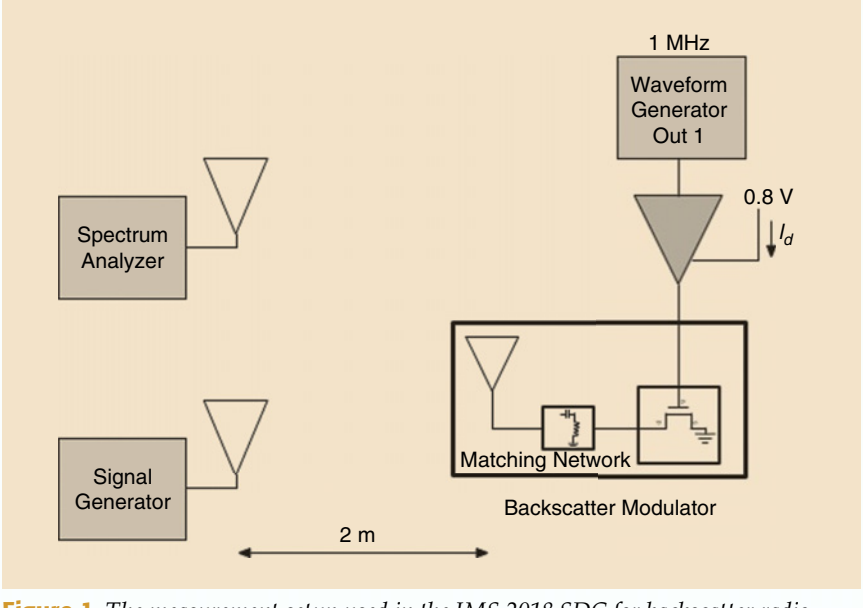

Figure 1. *The measurement setup used in the IMS 2018 SDC for backscatter radio.*

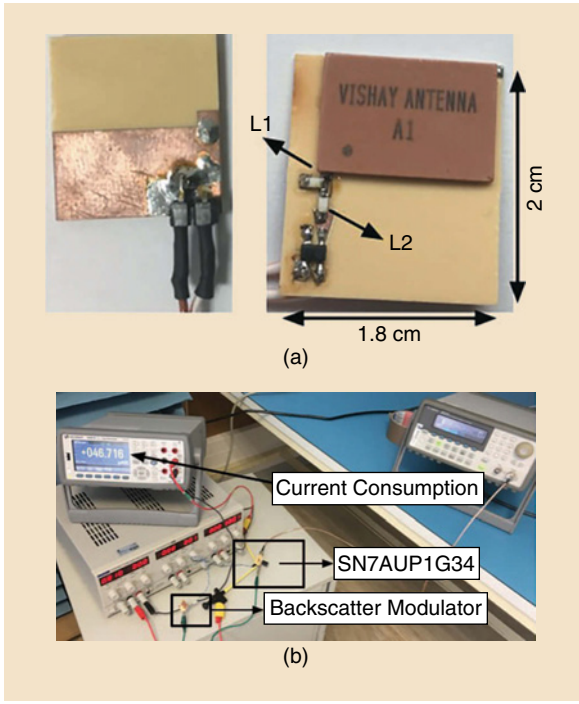

Figure 2. *(a) Photographs of the developed backscatter modulator. The element values are L1 = 22 nH, L2 = 27 nH; the substrate for the transmission lines is Astra MT77, thickness = 0.762 mm, $\varepsilon_r = 3.0$, and $\tan\delta = 0.0017$. (b) The setup for measuring the overall power consumption of the DUT.*

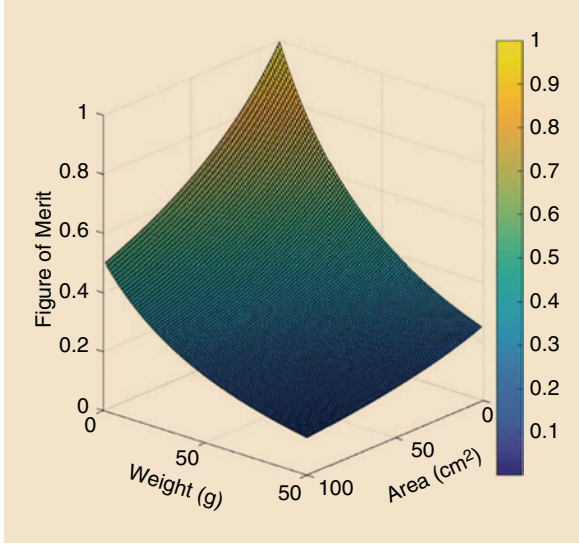

Figure 3. *The estimated FOM as function of area and weight.*

where $P_{RXi}, (i = 1, 2)$, is the power associated with the first sideband signal measured by the spectrum analyzer in the two power-transmitting experiments (i.e., power at 915 + 1 MHz) and $D1$, $D2$ are the sides of the smallest rectangle that can circumscribe the prototype circuit. The overall power consumption of the DUT, $P_{Ci}, (i = 1, 2)$, is calculated by measuring the power consumption of the driver (SN74AUP1G34), $P_{Ci} = V_{dd} \times I_d$. The variation of the power consumed by the tag with different transmitted power is negligible; thus, we considered $P_{C1} = P_{C2}$. From Figure 2(b), we present the measurement of the overall current consumption (46.7 μA), and, considering the V_{dd} of 0.8 V, we can calculate a power consumption of 37 μW.

Through (1), it was possible to estimate the FOM, which can be seen in Figure 3, as a function of area $(D1 \times D2)$ from 0 to 100 cm^2 and weight from 0 to 100 g. The power received in the spectrum analyzer can be estimated through

$$P_{RXi} = P_{TXi} + G_{TX} + G_{RX} + 2G_{\text{tag}} + 10\log_{10}\left(\frac{\lambda}{4\pi d}\right)^4 (\text{dBm}), \tag{2}$$

where G_{TX} and G_{RX} are, respectively, the gain of the transmitting and receiving antennas, G_{tag} is the gain of the tag antenna, d is the distance between the tag and the transmitting/receiving antennas, and λ is the radiation wavelength.

We considered the following values: $P_{TX1} = 25$ dBm, $P_{TX2} = 30$ dBm, $G_{TX} = 0$ dBi, $G_{RX} = 4$ dBi, $G_{\text{tag}} = -2.73$ dBi [16], and $d = 2$ m. The power consumed by the tag was considered to be 37 μW for both experiments ($P_{C1} = P_{C2}$). The developed circuit in this work is presented in Figure 2(a). The circuit is composed of a surface-mounted ceramic chip antenna (VJ5601M915MXBSR from Vishay) designed to operate at 915 MHz, an antenna-tuning circuit with two inductors, and an enhancement-mode pseudomorphic high-electron-mobility transistor (ATF54143 from Broadcom, chosen for its low gate-source drive capacitance), which is responsible for the ON and OFF switching. By changing the voltage presented to the gate of the transistor between 0 and 0.8 V, it is possible to change the phase of the reflection coefficient. In this work, binary PSK (BPSK) modulation was used to maximize the reflected power. The overall dimension of the circuit is 1.8×2 cm with a weight of 1.6 g.

To implement this circuit, several simulations were conducted. Figure 4(b) presents the reflection coefficient (S_{11}) simulated results when the voltage presented to the gate of the transistor varies from 0 V up to 0.8 V, for a 915-MHz operating frequency. To understand the behavior of the modulator at lower values of input power, these results were performed with a variation from −30 to 0 dBm of input power. As shown in Figure 4, it is possible to achieve 180° phase shift by simply switching the voltage at the gate of the transistor from 0 to 0.8 V. The simulations were performed with the Advanced Design System (ADS), and the schematic developed is presented in Figure 4(a).

After theoretically validating the transistor behavior, it was necessary to measure the antenna with the

tuning circuit to guarantee matching at 915 MHz. A simple printed circuit board was developed containing two inductors, the antenna, and a subminiature version A connector. A performance network analyzer (E8361C from Agilent Technologies) was used to measure the reflection coefficient (S_{11}); the results obtained, presented in Figure 5, show a reasonable match at the operating frequency. After these validations, the solution developed is presented in Figure 2(a).

Backscatter communication technology can facilitate the use of wearable devices and, when combined with wireless power transmission (WPT), increase the

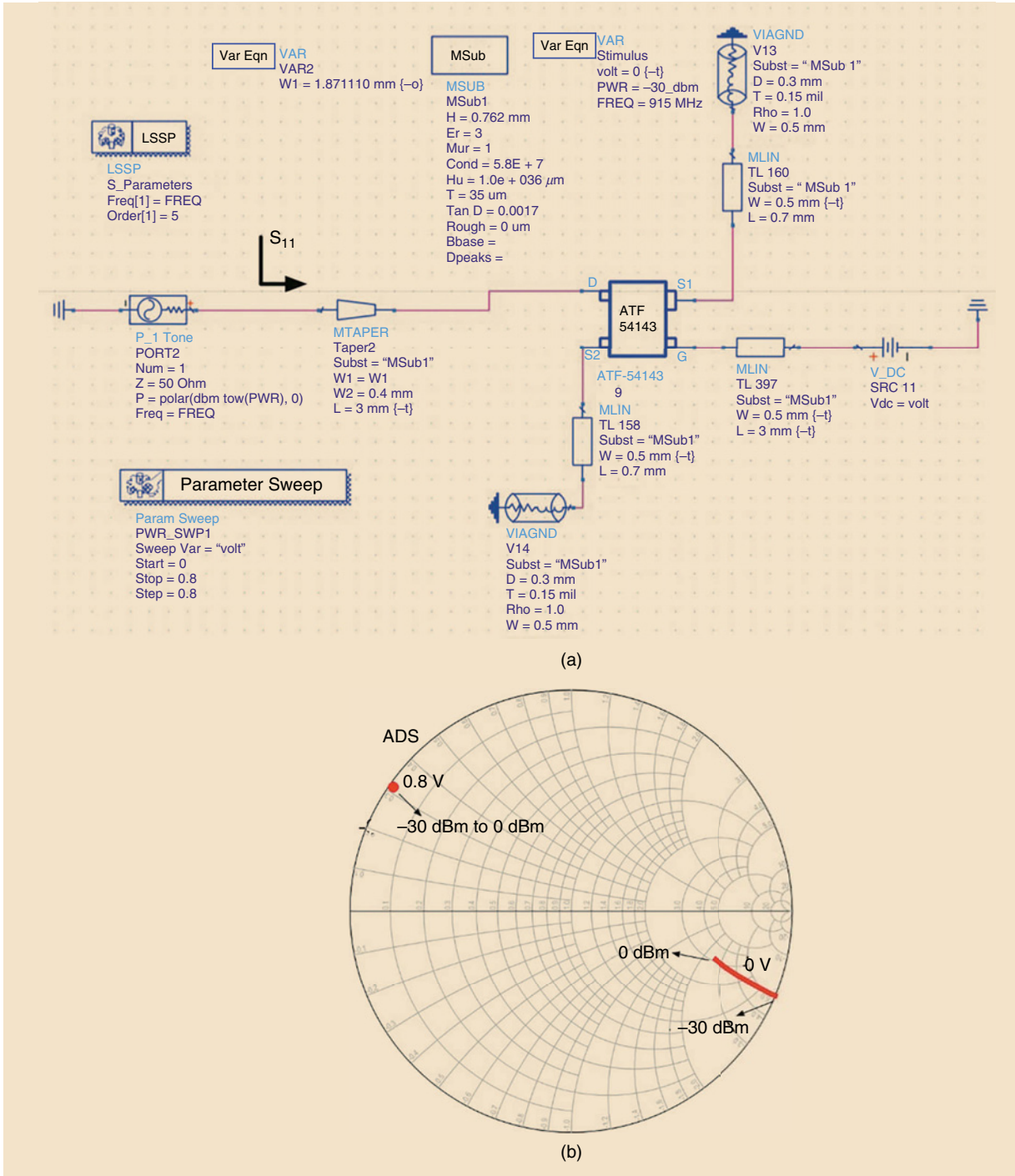

Figure 4. *Simulations of the backscatter modulator. (a) The proposed circuit developed with the ADS simulator. (b) The results obtained for S_{11} from the simulated circuit with two different voltages at the gate of the transistor (0 and 0.8 V). LSSP: large-signal S-parameters; Var Eqn: variables and equations component; MSub: microstrip substrate; ATF: Avago Technologies field-effect transistor.*

number of possible applications. Figure 6 shows the block diagram of a possible wearable device that can have sensing capabilities without requiring batteries. To power the microcontroller and the sensors, a rectifier (RF–dc converter) must be developed to convert the RF signals into dc energy.

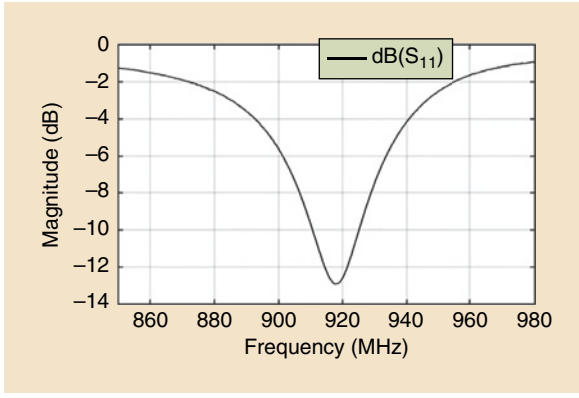

Figure 5. *The measured S_{11} of the chip antenna.*

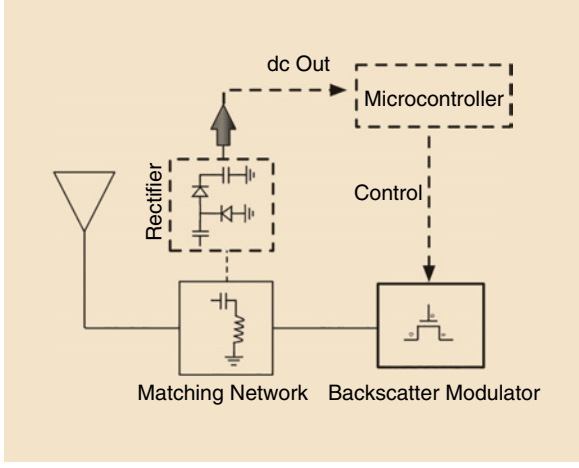

Figure 6. *A block diagram of a battery-free wearable device.*

Figure 7. *The backscatter modulator embedded into a watch.*

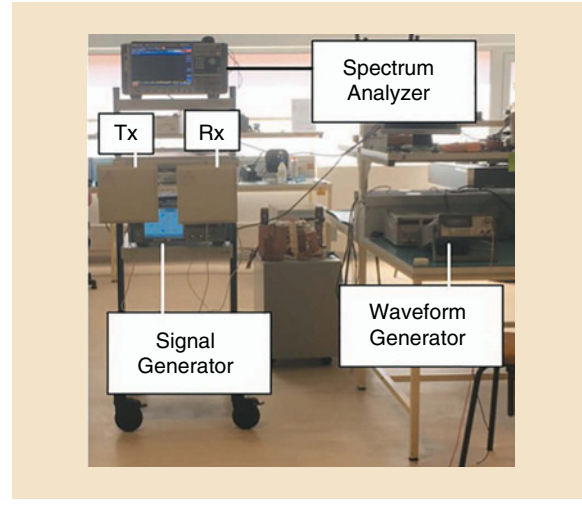

Figure 8. *The laboratory measurement setup. Tx: transmitter; Rx: receiver.*

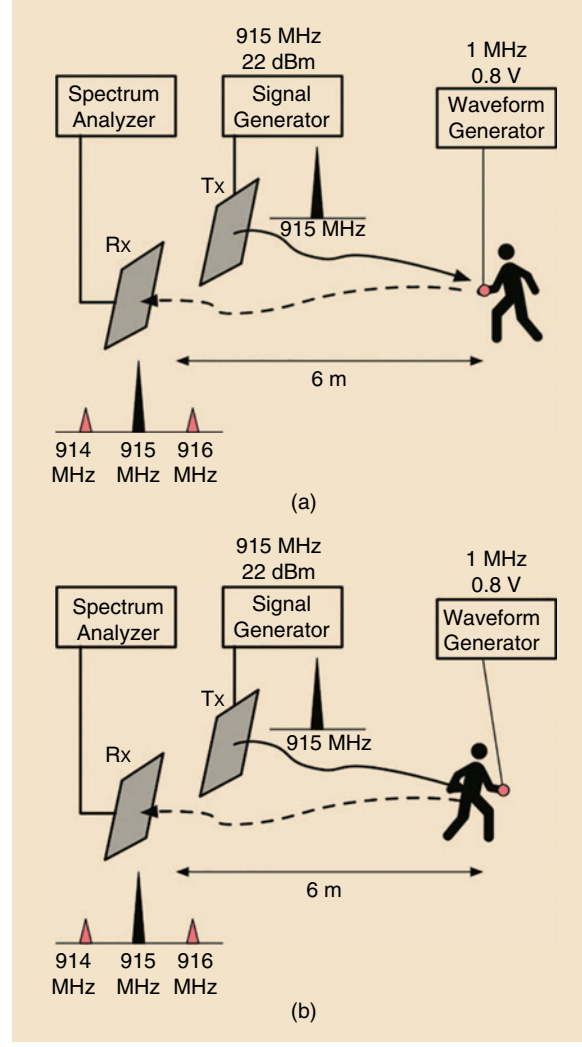

Figure 9. *The two different scenarios used to measure the backscatter modulator embedded into the watch. In (a), the person is shown in front of the setup. In (b), the person is turning his or her back to the setup.*

DUT Performance in Wearable Applications

To evaluate the behavior of the backscatter modulator as a wearable device, we inserted the developed circuit presented in Figure 2 into a wristwatch, as seen in Figure 7. The two wires coming out of wristwatch connect to the waveform generator, which produces an 0.80-Vpp, 1.0-MHz square wave signal. In a real scenario, this modulating signal would be replaced by the bit stream generated by the microcontroller containing the desired sensing information.

The setup used for the experimental measurements can be seen in Figure 8. It is composed of two commercial antennas (ALR-8610-AC from Alien), a signal generator (SMW200A from Rohde & Schwarz) to generate the continuous wave at 915 MHz, a spectrum analyzer (FSW8 from Rohde & Schwarz) to obtain the reflected wave at 915 ± 1 MHz, and a low-frequency waveform generator (33250 A from Agilent Technologies) to generate the 1.0-MHz square-wave signal.

To evaluate the proposed wristwatch presented in Figure 7, we conducted two different scenarios, both shown in Figure 9. The wristwatch with the backscatter modulator inside was attached to a person's wrist, and several measurements were taken while he or she was moving. In the first scenario, the person moved away from the antennas with his or her back turned to them. In the second scenario, the person moved toward the antennas while facing them. The power transmitted from the signal generator was at 915 MHz was 22 dBm. Considering the losses introduced by the antenna cables (3 dB) and the gain of the antenna (estimated at 5.5 dBi without a cable and 4 dBi with a cable), the equivalent isotropic radiated power was estimated to be 23 dBm (the antenna used with a cable). The power obtained at the modulation frequency (916 MHz) in the spectrum analyzer for the two different scenarios is presented in Figure 10. In Figure 11 we present two results for a distance of 4 m in both scenarios (front and back). Because BPSK modulation was used and also because the bandwidth needed to transfer such a low bit rate is very small, all the signal powers being received can be decoded by any general-purpose receiver.

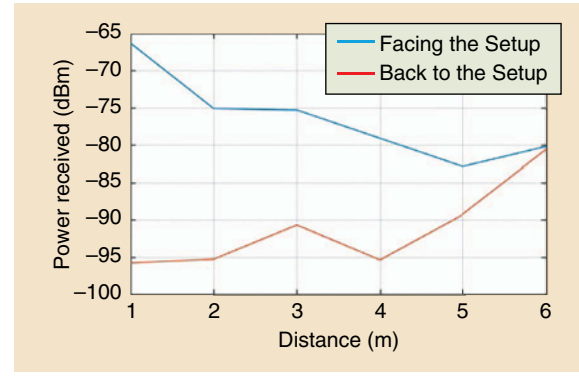

Figure 10. *The power received by the spectrum analyzer at 916 MHz.*

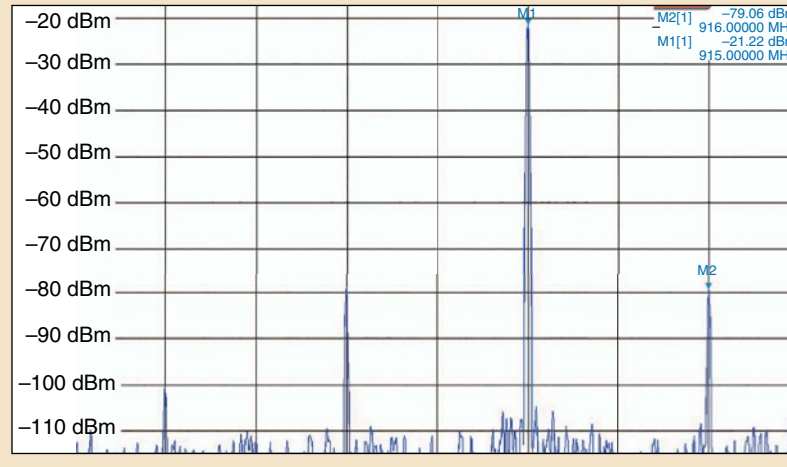

Figure 11. *The measurement results with the person wearing the DUT positioned 4 m from the transmitter/receiver. In (a), the person faces the setup. In (b), the person has his or her back to the setup.*

Backscatter communication technology can facilitate the use of wearable devices and, when combined with wireless power transmission, increase the number of possible applications.

An analysis of Figure 10 shows that, as the distance increases, the power received at the modulation frequency decreases. A comparison of the received values for the two scenarios indicates that, when the person has his or her back turned to the reader, the power received is lower due to some body blockage. Moreover, at higher distances the received power is similar in both scenarios, mainly due to the multipath effects.

Conclusions

The proposed work presents a light, compact, and efficient backscatter modulator that can be used in wearable devices. Although tests were performed in a laboratory environment, the device implanted in a wristwatch was used in a realistic application. These results prove the concept, demonstrating that the technology can be implemented in real wearable devices, which are increasingly in use.

This approach has the advantage of extending the wearable device's battery. This kind of communication consumes less power than any other. Besides that, this technology can be combined with WPT techniques to enable batteryless devices.

By using this approach, a considerable distance between the reader and the device was achieved using conventional values for the transmitted power and sensitivity. The distance could be extended by increasing the transmitted power or antenna gain (below the values of regulation). Another way to enable transmission over longer distances is to improve the sensitivity of the receiver. For example, long-range communication modules with sensitivity as low as –146 dBm might be used in such devices.

Acknowledgments

We acknowledge the effort put into the development and execution of this International Microwave Symposium Student Design Competition. We also thank Rhode & Schwarz for providing the equipment for the competition, as well as all the members of Technical Committee 24 of the IEEE Microwave Theory and Techniques Society for this amazing organizational achievement. This work is supported by the European Regional Development Fund through the Competitiveness and Internationalization Operational Programme of the Portugal 2020 framework, Project MOBIWISE (POCI-01-0145-FEDER-016426). It is also funded by the Faculdade de Ciéncias de Tecnologia/Ministereo da Educação e Ciéncias of Portugal through national funds. The source of cofunding was a European Fund for Regional Development–PT2020 partnership agreement under the project UID/EEA/50008/2013.

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2018 Student Design Competition Winners IMS

High-Efficiency Power Amplifier

Striving for Efficiency

Wooseok Lee, Jaekyung Shin, Hansik Oh, Taewan Kim, Kimok Kim, Keum Choel Hwang, Kang-Yoon Lee, and Youngoo Yang

This article presents the design and validation for the high-efficiency class-E power amplifier (PA) that won first place in the high-efficiency PA for 475 kHz Student Design Competition held during the 2018 IEEE Microwave Theory and Techniques Society International Microwave Symposium (IMS 2018) in Philadelphia, Pennsylvania. Participants were required to implement and evaluate their own PAs. The team that achieved the highest drain efficiency while satisfying the conditions of the competition rules was the winner. The conditions of this year's competition were as follows:

- The output power should be 10–11 W into a 50-Ω load at 475 kHz from a 12-V power supply.
- The power supply supplies only 12 V.
- This design will use a single IRF510 power metal–oxide–semiconductor field-effect transistor (MOSFET).
- The input from the external continuous-wave signal source is 0 dBm.
- The input standing-wave ratio (SWR) must be lower than 2:1 relative to 50 Ω.
- The harmonics must be lower than 40 dBc (up to 1 GHz).
- The nonharmonic spurs must be fewer than –70 dBc (10 kHz to 1 GHz).
- There will be no oscillation if the signal input is removed.
- No commercial subassemblies are allowed.

The 630-m amateur radio band ranges from 472 to 479 kHz and is allocated by the International

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Telecommunication Union for amateur service. Amateur stations must have a maximum effective isotropic radiated power (EIRP) of 1 W. Stations more than 800 km away from the borders of certain countries are allowed to have an EIRP of up to 5 W. This band range was formally assigned at the 2012 World Radio Communication Conference. Since then, various studies have been undertaken to optimize radio transmitters for amateur service [1].

RF power transmitters require high efficiency to prevent thermal problems and avoid safety concerns. The PAs in power transmitters consume a great deal of dc power to generate high RF power, so PA efficiency is very important for the performance of the entire system. Various studies have been conducted with the goal of increasing PA efficiency. Class E and class F are representative high-efficiency PA classes [2]–[5]. Class-F PAs can theoretically deliver 100% efficiency by appropriately terminating harmonics, which requires very large, complex circuits. However, class-E PAs have a very simple circuit based on a transistor switching operation and can theoretically deliver 100% efficiency as well. Because class-E PA switching operation requires an output capacitor, which may include the output parasitic capacitor of the transistor, its frequency characteristics can be a little better than those of other switching-mode PAs. Because of these advantages, class-E PAs have been widely used in power transmitters [2]–[14].

To achieve high efficiency from a class-E PA, the lumped elements in the load network must have a high quality factor (Q factor) [6]–[9]. Specifically, the inductor in the series resonant circuit is very important for reducing current loss and attenuating harmonics. In addition to high-Q lumped components, additional harmonic filters can be deployed to further suppress the harmonics [10]–[13]; e.g., a quarter-wave transmission line is sometimes used at the output network [12], [13]. However, it is difficult to use a quarter-wave line at so low a frequency as 475 kHz due to its large size. In another approach, a class-D PA using a push–pull configuration has been reported [14]. Although this configuration can be effective in suppressing even-order harmonics, additional input and output baluns can make the circuit bulky and cause additional loss.

This article presents a two-stage class-E PA for the 630-m amateur radio band (475 kHz). Using the implemented high-Q inductors based on enamel-coated copper wire and ferrite cores, the designed class-E PA exhibited high efficiency and complied with all conditions required by the competition. To address the harmonics requirement, a second-harmonic resonant filter was applied to the load-matching network. The design procedure and details as well as the measured performances of the two-stage class-E PA are described in the following.

Overall Circuits

Figure 1 is a schematic of the proposed two-stage class-E PA. The two stages consist of two power MOSFETs, Fairchild's FDMC86248 and Vishay's IRF510, for the drive and main stages, respectively. The main stage is designed for class-E operation using a shunt capacitor (C_{SH}), a series LC resonance circuit with C_R and L_R, and a simple L-section matching network with L_M and C_M.

The optimum impedances for the drive and main stages were obtained using source- and load-pull simulations. The source and load impedances of the main stage are extracted as 800 Ω and $7 + j3$ Ω, respectively. Because the drive stage performs adequately with a load impedance of 800 Ω (which is the same as the input impedance of the main stage), interstage impedance matching is not required. The source impedance of the drive stage was determined to be about 100 Ω, which requires a 100-Ω shunt resistor to comply with an input SWR condition lower than 2:1.

The ideal value of the shunt capacitor (C_{SH}) was calculated as 8.5 nF using an equation given by [2]. However, the calculated value must be refined because the transistor includes an output parasitic capacitance. The shunt capacitor (C_{SH}) and the load impedance must be simultaneously optimized for the best simulated performance. The series LC resonance circuit provides a short circuit at the fundamental frequency (ω_C) and rejects the

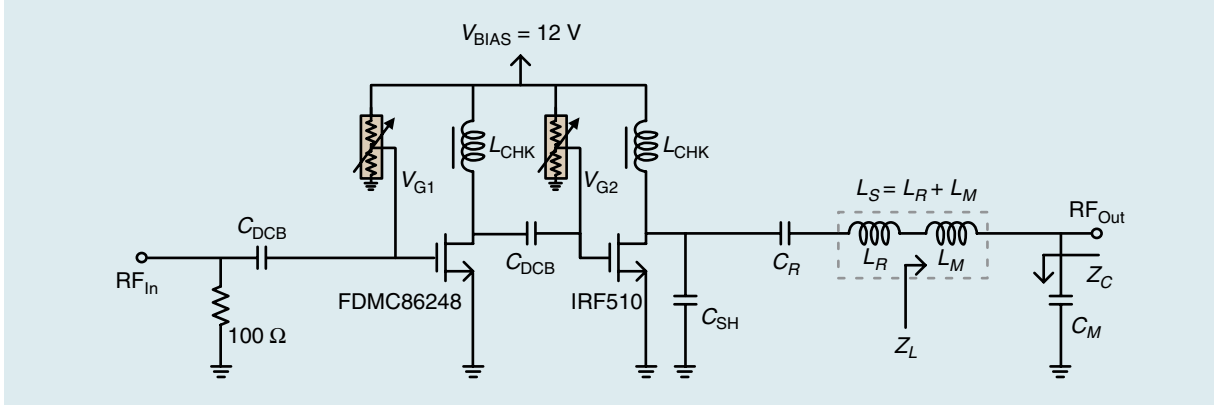

Figure 1. *A schematic of the overall two-stage class-E PA.*

harmonic frequencies. The value of the inductor (L_R) is selected first, assuming the implementation conditions to be 11.8 μH; the capacitor (C_R) can be selected later as 9.6 nF to achieve a resonance at the fundamental frequency. In addition, an L-section matching network using L_M and C_M comes after the resonance circuit. The inductor of the series resonance circuit, L_R, and an inductor for the matching network, L_M, can be merged to form a single series inductor of L_S. The gate biases of the drive and the main stages can be supplied from a single supply voltage of 12 V through potentiometers. Figure 2 presents a trajectory for the fundamental impedance matching using an L-section matching network. The optimum load impedance, Z_L, of $7 + j3\,\Omega$ can be matched using a series inductor, L_M, of 8.2 μH and a shunt capacitor, C_M, of 16.6 nF.

Second-Harmonic Resonant Filter

Because the second harmonic generally has the largest magnitude among all harmonics and the load network of the class-E PA can better suppress higher-order harmonics, it is often necessary to further suppress the second harmonic. A schematic of the second-harmonic resonant filter, which replaces the shunt capacitor (C_M) in the matching network, is shown in Figure 3. The shunt capacitor, C_M, at the load-matching network can be replaced by a series LC network with an inductor (L_2) and a capacitor (C_2), as shown in Figure 3.

At the fundamental frequency (ω_C), the impedance of the shunt capacitor, C_M, must be the same as the impedance of the second-harmonic resonant filter:

$$Z_C(\omega_C) = j\omega_C L_2\left(1 - \frac{1}{\omega_C^2 C_2 L_2}\right) = \frac{1}{j\omega_C C_M}. \tag{1}$$

After reorganizing (1), a relationship between C_M and components in the second-harmonic resonant filter is obtained as

$$C_M = \frac{C_2}{1 - \omega_C^2 C_2 L_2}. \tag{2}$$

At the second-harmonic frequency ($2\omega_C$), the second-harmonic resonant filter must have a resonance to exhibit a minimum impedance for the second-harmonic frequency. From this condition, we can derive another relationship for the component values of the second-harmonic filter:

$$Z_C(2\omega_C) = j2\omega_C L_2\left(1 - \frac{1}{(2\omega_C)^2 C_2 L_2}\right) = 0 \tag{3}$$

or

$$\omega_C = \frac{1}{2\sqrt{L_2 C_2}}. \tag{4}$$

From (2) and (4), C_2 can be found exactly using C_M as

$$C_2 = \frac{3}{4} C_M. \tag{5}$$

Now, L_2 can be obtained as

$$L_2 = \frac{1}{4\omega_C^2 C_2}. \tag{6}$$

Using (5) and (6), exact values of C_2 and L_2 can be found from the value of C_M. Because C_M was obtained as 16.6 nF, the values of C_2 and L_2 are found to be 12.5 nF and 2.25 μH, respectively.

Figure 4(a) and (b) shows the simulated S parameters of the load-matching network, with and without the second-harmonic resonant filter, using the calculated values of C_2 and L_2. The simulated S_{22}s, shown in Figure 4(a) on the Smith chart, show exactly the same values at the center for the fundamental frequency but show very different values for the second-harmonic

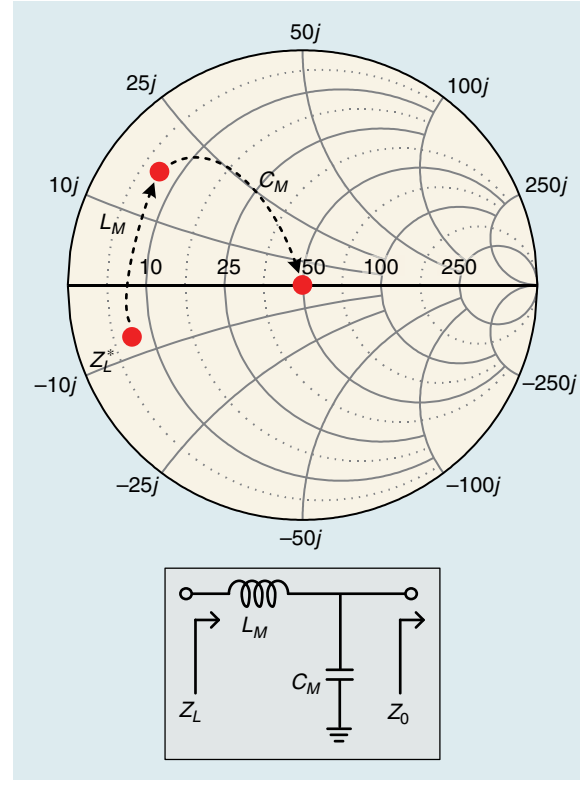

Figure 2. *The fundamental impedance matching using an L-section matching network.*

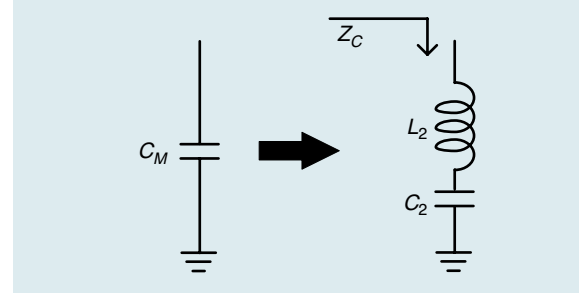

Figure 3. *A second-harmonic resonant filter from a shunt capacitor at the matching network.*

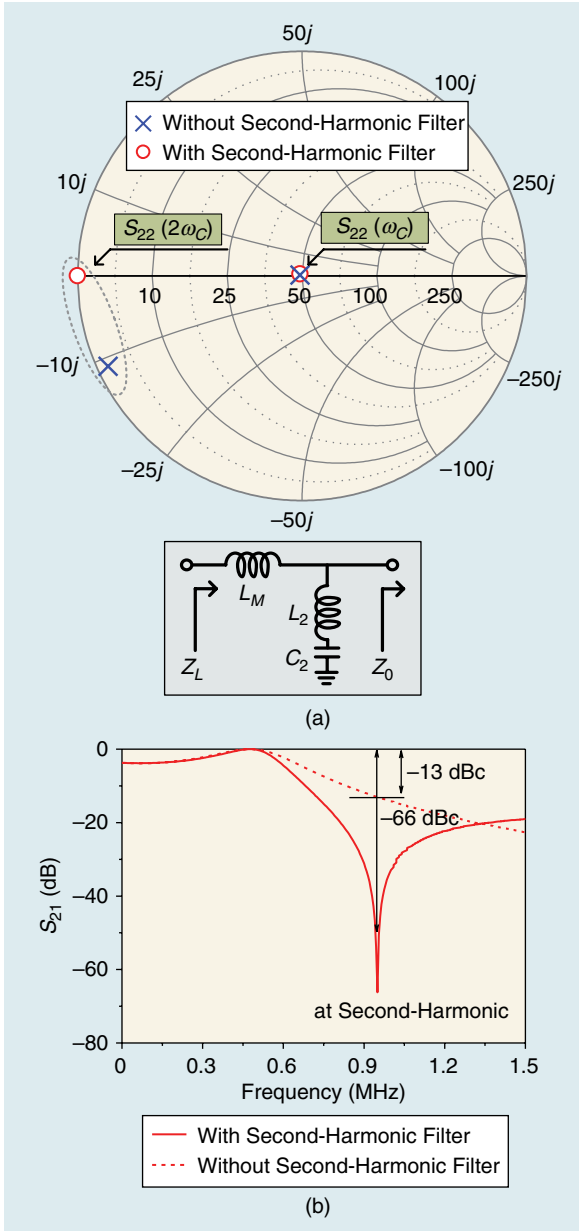

Figure 4. *The simulated S parameters of the load-matching network with the second-harmonic resonant filter: (a) S_{11} and (b) S_{21}.*

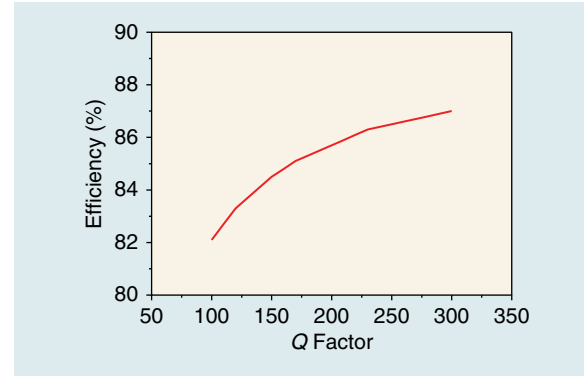

Figure 5. *The simulated efficiency according to the Q factor of the series inductor (L_S).*

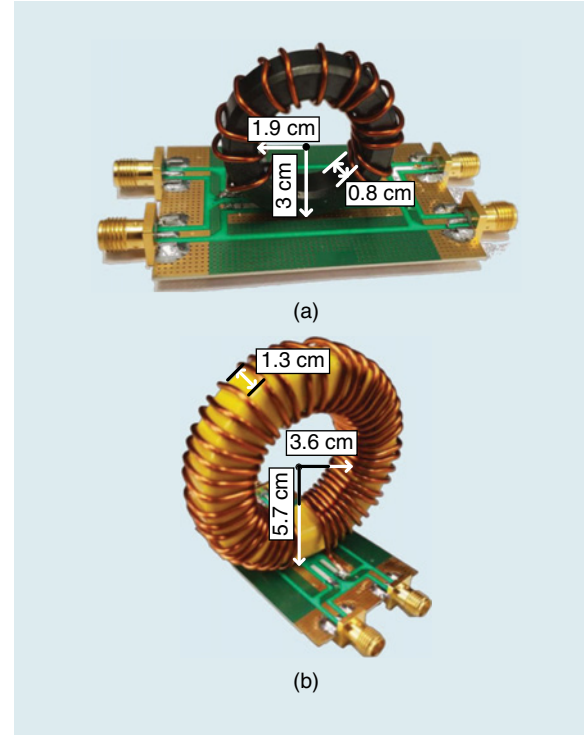

Figure 6. *Photographs of the implemented high-Q inductors: (a) L_{CHK} and (b) L_S.*

frequency with and without the second-harmonic resonant filter. With the second-harmonic filter, the simulated S_{22} is exactly at –1, or the output impedance is at 0, which results in very good rejection of the second harmonic, as shown in Figure 4(b) from the S_{21} plot. Ideally, we can have second-harmonic suppression of about –66 dBc with the second-harmonic resonant filter.

High-*Q* Inductors

Figure 5 exhibits the simulated efficiency according to the *Q* factor of the series inductor (L_S) at the load of the main stage of the class-E PA. As the *Q* factor increases, the efficiency increases accordingly. From this fact, one can deduce that it is very important to implement a high-*Q* inductor to achieve high efficiency for the class-E PA. Two types of inductors, L_S and L_{CHK}, were implemented in-house to achieve a high-*Q* factor.

Figure 6 shows photographs of the implemented high-*Q* inductors. The RF choke inductor (i.e., L_{CHK}) must have very low resistance at dc and very high inductance to block the signal leakage. An inductance of 300 μH for RF choke at 475 kHz was implemented using a ferrite core with high permeability. For L_{CHK}, we used a ferrite core, TDK's PC40 with an outer diameter of 3.0 cm, an inner

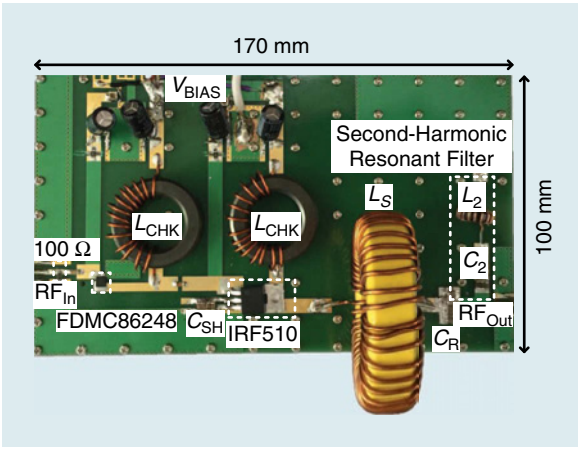

Figure 7. *The implemented two-stage class-E PA.*

TABLE 1. The values and information for the components used in the two-stage class-E PA.

Component	Value	*Q* factor	Vendor
L_S	20 μH	298	In-house
C_R	9.12 nF	>350	Samsung
C_{SH}	13.2 nF	>350	Samsung
L_2	1.5 μH	60	ABCO
C_2	14.1 nF	>350	Samsung
L_{CHK}	300 μH	150	In-house
C_{DCB}	330 nF	>350	Samsung

diameter of 1.9 cm, a height of 0.8 cm, and a permeability of 2,300 H/m. Enamel-coated copper wire having a diameter of 1 mm was wound 14 turns around the core to generate an inductance of 300 μH. The measured resistance at dc was as small as 0.01 Ω. A photograph of the implemented L_{CHK} is shown in Figure 6(a).

For the series inductor (L_S, 20 μH), an inductor for series resonance (L_R, 11.8 μH) and an inductor for load-impedance matching (L_M, 8.2 μH) were merged. The ferrite core is Micrometals' T225-8/90, with an outer diameter of 5.7 cm, an inner diameter of 3.6 cm, a height of 1.3 cm, and a permeability of 35 H/m. Enamel-coated copper wire with a diameter of 1.5 mm was wound 44 turns around the core to realize an inductance of 20 μH. The measured *Q* factor of the L_S was as high as 298.

Implementation and Measurement Results

Figure 7 shows the implemented two-stage class-E PA on a printed circuit board based on FR4 with a relative permittivity of 4.7. The circuit size is 170 × 100 mm^2. The second-harmonic resonant filter was fabricated using an ABCO 1.5 μH inductor, which exhibits the closest to the calculated value among off-the-shelf components. Accordingly, the value of C_2 must be selected as 14.1 nF to provide the same reactance at the fundamental

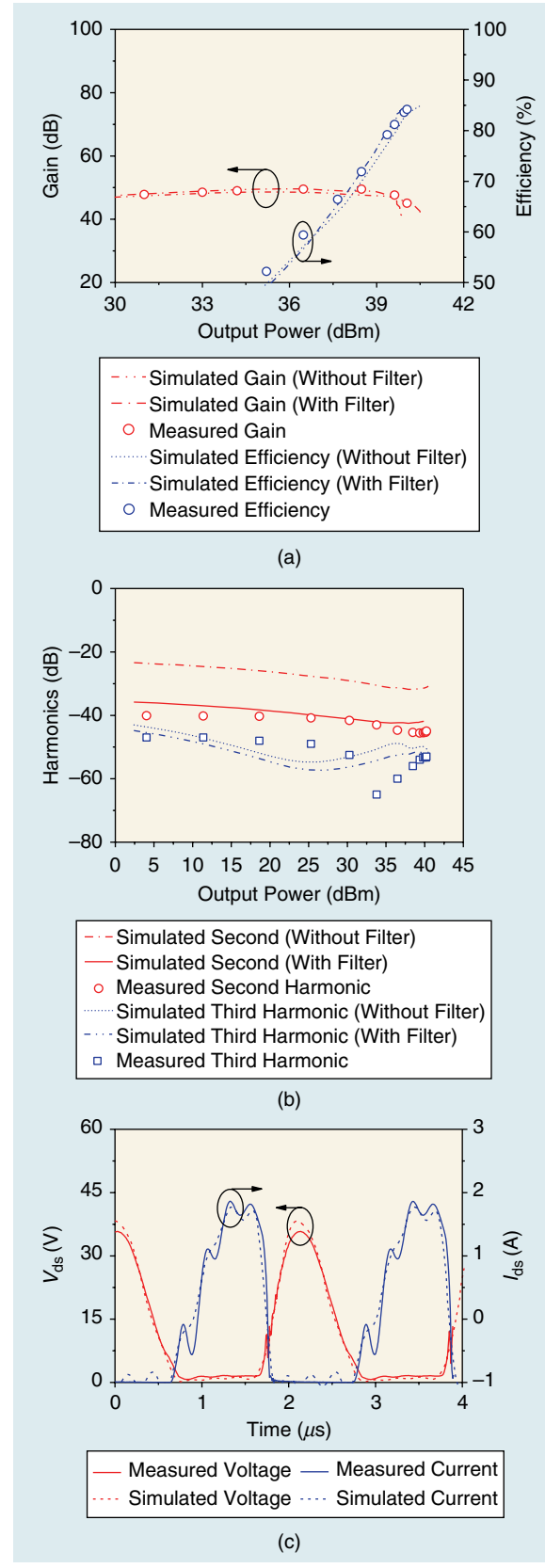

Figure 8. *The simulated and measured results of the two-stage class-E PA: (a) gain and efficiency, (b) harmonics, and (c) waveforms.*

TABLE 2. The performance of the two-stage class-E PA as compared to previous works.

Reference	Frequency (MHz)	P_{out} (dBm)	Efficiency (%)	V_{DD} (V)	Harmonic (dBc)	Stage	Device	Structure	Feature
[9]	6.78	38.8	90.8	20	N/A	1	LDMOS	Class E	High-Q inductor
[11]	1.0	33.4	80.4*	12	N/A	1	MOSFET	Class E	Parallel LC resonator
[14]	13.56	44.4	84.6	28	−50.3	1	MOSFET	Class D	Transformer and harmonic filter
This work	0.475	40.3	84.7	12	−45.2	2	MOSFET	Class E	Second-harmonic resonant filter

*: calculated by P_{OUT}/P_{dc}.
LDMOS: laterally diffused MOSFET.

frequency as C_M does. Sufficient second-harmonic suppression was achieved using the implemented resonant filter to satisfy the competition's conditions. The values of and information about the components used for the two-stage class-E PA are presented in Table 1.

Figure 8(a) shows the simulated and measured gain and efficiency performances, Figure 8(b) the simulated and measured harmonics, and Figure 8(c) the simulated and measured waveforms of the two-stage class-E PA at the 475-kHz frequency. As the figure illustrates, the simulated and measured performances are in good agreement. The simulated and measured second-harmonic results clearly show that the implemented second-harmonic resonant filter works well enough for the PA to have a harmonic distortion level lower than −40 dBc. Because of the loss caused by L_2 in the second-harmonic resonant filter, the simulated efficiency of the PA was reduced by about 1% compared to that of the PA without the second-harmonic resonant filter.

Both the driver and the main stages are biased for class-C operating points. As shown by the measured results, the implemented two-stage class-E PA exhibited a high power gain of 40.3 dB, a peak output power of 40.3 dBm, and an efficiency of 84.7% at the 475-kHz frequency. In addition, the two-stage class-E PA showed a second-harmonic distortion of –45.2 dBc at an output power of 40.3 dBm. Table 2 compares the performance of the two-stage class-E PA with those of previously published class-E PAs in Table 2.

Conclusions

In this article, a two-stage class-E PA with a second-harmonic resonant filter was proposed and implemented for the 475-kHz band. High-Q inductors were implemented in-house using enamel-coated copper wires and ferrite cores with high permeability for high efficiency. The second-harmonic resonant filter was adopted at the output matching network to further improve the second-harmonic distortion. The implemented class-E PA showed a high gain of 40.3 dB, a high efficiency of 84.7%, and an excellent second-harmonic distortion of −45.2 dBc at an output power of 40.3 dBm.

Acknowledgment

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2018 Student Design Competition Winners IMS

High-Sensitivity Fast-Response Motion-Sensing Radar

(Micro)Metering with Microwaves

Fabian Michler, Benedict Scheiner, Fabian Lurz, Robert Weigel, and Alexander Koelpin

Over the last several years, short-range, noncontact microwave radar systems for industrial and medical applications have received significant attention for several reasons [1], [2]. First, today's RF chips are more efficient and smaller than comparable chips of a few years ago. Second, the high demand for new sensor systems in health-care, automotive, and industrial applications, especially as the field of smart factories emerges, has boosted development of ultralow-cost radar modules for the mass market [3], [4].

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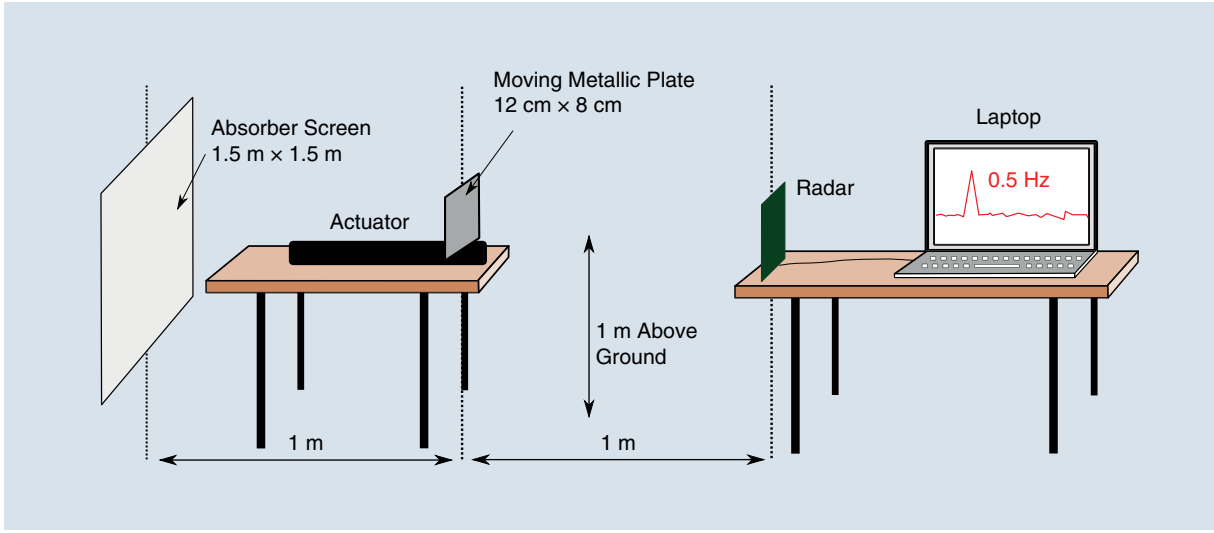

Figure 1. *The measurement setup during the competition.*

TABLE 1. The score calculation for each correct detection.

Correct Detection	Score
1	$70 - 5 \cdot \log(W_R) - 2 \cdot \log(P_{DC})$
2	$5/(f_d \cdot t_d)$
3	$10/(f_d \cdot t_d)$
4	$15/(f_d \cdot t_d)$
5	$20/(f_d \cdot t_d)$

To motivate students and encourage new approaches in the design of short-range radar systems, the IEEE Microwave Theory and Techniques Society Technical Coordinating Committees 10 and 20 sponsored the fourth annual Student Design Competition (SDC) on high-sensitivity, fast-response motion-sensing radar systems. The competition took place at the 2018 International Microwave Symposium (IMS) held in Philadelphia, Pennsylvania. This article presents the winning design and prototype. The system is designed to achieve the highest possible figure of merit (FOM) by sensing relative displacements down to 10 μm while consuming less power and achieving faster performance than competing systems. Because it incorporates a frequency of the 24-GHz industrial, scientific, and medical band into a cost-efficient design, this system is also attractive for many industrial and medical applications.

Scenario and FOM Analysis

The design followed the SDC rules (see [5] for details), and the prototype was measured during the competition using the measurement configuration shown in Figure 1. The distance between the radar system and target was specified to be 1 m. Using a precise actuator, the target could be moved in several known amplitudes and frequencies (0.4, 0.5, 0.6, 0.7, 0.9 Hz), which can be assumed as almost sinusoidal. The amplitudes of this oscillation are 2.0 mm, 1.0 mm, 0.5 mm, 100 μm, and 10 μm and were applied in this order during the competition. The oscillation frequency of the metallic plate chosen randomly by the judges was the parameter to be sensed by the teams. The score of each team was calculated using the equations given in Table 1.

For the score of the first correct detection, only weight W_R and power consumption P_{DC} were included; for every subsequent measurement, only response time t_d and detected frequency f_d were taken into account as a product in the equations' denominators. With an increased number of correct detections, the scaling factor also rose. The most important difference in requirements compared to last year's FOM was that for the 2018 competition a logarithm was applied to W_R and P_{DC}, which placed less importance on reducing weight and power consumption [6].

However, as Table 1 indicates, a fast response that includes the correctly detected frequency for all amplitudes was the main system design parameter, even as maintaining the lowest weight possible remained an important factor. Once a system with a resolution better than 10 μm is developed, the weight and power consumption can be trimmed as much as possible. So, in contrast to the winning ultralow-power radar design of the 2017 SDC, which was presented in [7], a new radar front end tailored to the new FOM was designed.

System Design

In the following, we introduce the important parts of the system, first introducing the fundamentals of

continuous-wave radars and then investigating the analog parts of the system in terms of signal generation, link budget, and antenna, as well as baseband signal conditioning. Moreover, the choice of the digital building blocks will be explained.

A Continuous-Wave Radar

The proposed radar system operates at a single frequency f in pulsed operation mode to reduce average energy consumption. A radar transceiver (Figure 2) generates and transmits an RF signal, which is reflected by the target. In this case, the target is a moving metal plate. Hence, the signal received by the radar system is a delayed and attenuated version of the transmit (Tx) signal; i.e., a phase shift $\Delta\varphi(t)$ occurs between the Tx and receive (Rx) signals, which can then be used to compute the relative target displacement $d(t)$ because the propagation speed in free space c_0 is known:

$$d(t) = \frac{1}{2} \cdot \frac{c_0}{f} \cdot \frac{\Delta\varphi(t)}{2\pi}. \tag{1}$$

To determine the required phase shift $\Delta\varphi(t)$, the downconverter of the transceiver mixes an amplified version of the Rx signal with its local oscillator signal (which is a copy of the Tx signal), delayed by 0° and 90°, respectively. The resulting signals, denoted as the in-phase (I) and quadrature (Q) components, form the complex baseband signal $B(t) = I(t) + jQ(t)$. The argument of the complex voltage then equals the desired phase difference $\arg(B) = \arctan(Q(t)/I(t)) = \Delta\varphi(t)$.

Signal Generation

To achieve a high precision for the displacement measurement, the transceiver's oscillator must be stabilized to minimize its phase noise; hence, the radar transceiver provides an output port for the Tx signal, which is divided in frequency. This signal is fed to an integrated phase-locked loop (PLL), which compares the signal to a reference from a temperature-compensated crystal oscillator (TCXO) and generates a control voltage proportional to the phase error. This control voltage passes through the loop filter and corrects the transceiver's RF signal.

The losses in the signal path are the free-space propagation losses from the system to the target and vice versa, including the reflectivity of the target.

A simplified block diagram of the monolithic microwave integrated circuit (MMIC) used in the system is shown in Figure 3. The output of the frequency divider f_{DIV} as well as the input for the tuning voltage V_{tune} can be seen. Using a polyphase filter, the reference signal is split up and shifted by 90° and 0°, respectively, so the I and Q portions of the signal can be received by mixing both reference signals with the amplified, backscattered RF signal. Because the proposed system requires the generation of only a single frequency, an integer-N PLL was chosen over the fractional-N PLL considering that an integer-N PLL does not contain a sigma–delta modulator and so offers superior noise performance. Simulations with the ADISimPLL tool from Analog Devices have shown that a phase noise of –82 dBc/Hz at an offset frequency of 10 kHz could be achieved at a fast lock time of 20 μs.

Baseband Amplification and Filtering

In the next step, the downconverted baseband signals must be filtered and amplified. Two first-order resistor–capacitor filters were used before and after an operational amplifier. The resulting bandwidth of these filters is a crucial parameter for the sensing

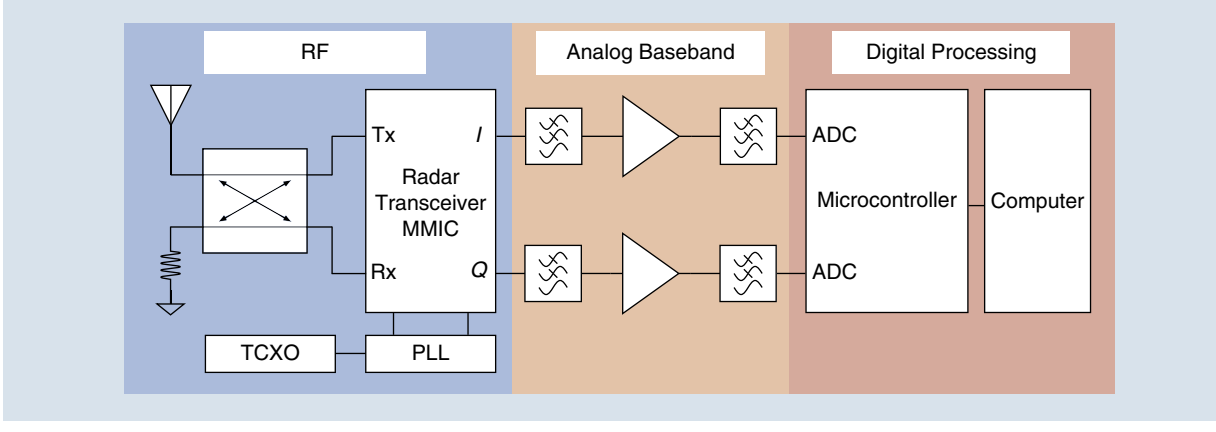

Figure 2. *A block diagram of the radar system.*

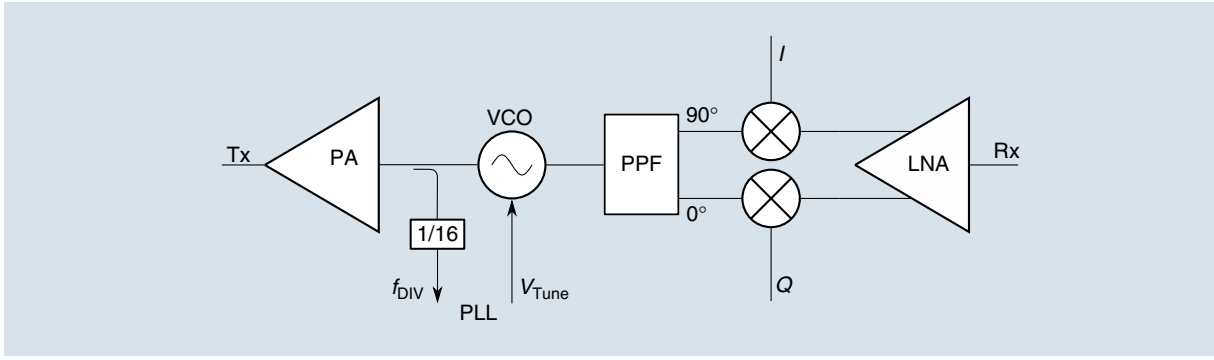

Figure 3. *A simplified block diagram of the 24-GHz radar transceiver [8]. PA: power amplifier; PPF: polyphase filter; LNA: low-noise amplifier.*

system. While a smaller bandwidth reduces the baseband noise and so improves measurement precision, it increases the time constant of the signal path, which means the pulses must be longer to allow for settling of the voltages, thus increasing the system's energy consumption. For the given phase noise achievable with the chosen combination of PLL and voltage-controlled oscillator (VCO), the resulting root-mean-square (rms) error contributions to the displacement measurement of fewer than 3 nm could be calculated using the formula from [9] and [10], if baseband bandwidths of 10 kHz or smaller are used for a target distance of 1 m. This shows that the achieved phase noise is sufficiently low and will allow the measurement of displacement amplitudes down to 100 μm, if the filters are properly designed. The chosen bandwidth for each filter must be slightly larger to achieve the desired overall baseband bandwidth because of the two filter stages before and after amplification.

Microcontroller and Timing

The amplified and filtered baseband voltages are then digitized using the microcontroller's analog-to-digital converters (ADCs). Oversampling further reduces the measurement noise through averaging. The microcontroller also controls the active parts of the system. As explained previously, the system operates in a pulsed mode to reduce average power consumption. Thus, the microcontroller activates different parts of the system individually and only when they are needed. Otherwise, they are put into sleep mode to save energy.

TABLE 2. The estimated link budget of the radar system.

VCO	6 dBm
Coupler	−3 dB
Antenna	+15 dBi
Path and target	−62 dB
Antenna	+15 dBi
Coupler	−3 dB
Receiver	−32 dBm
Conversion gain	+20 dB
Baseband voltage	80 mV

Link Budget and Antenna

To derive the antenna design parameters, the entire system's link budget must be estimated, as shown in Table 2. The output power generated by the radar transceiver is specified to be 6 dBm, which can be reduced to about 3 dBm by the coupler that separates Tx and Rx signals. The planar branchline coupler with a terminated port is very compact and still shows a good isolation between the Tx and Rx ports of about 25 dB, according to field simulations.

The losses in the signal path are the free-space propagation losses from the system to the target and vice versa, including the reflectivity of the target. These sum to a path loss of 62 dB [11] and finally lead to an Rx power of –62 dB, again taking into account the directional coupler and assuming an omnidirectional antenna. The use of a monostatic antenna with a gain of 15 dBi will increase the Rx signal power to a level of –32 dBm. The downconversion in the receiver ultimately introduces a voltage gain of 20 dB, leading to baseband voltages of approximately 80 mV; these can then be further amplified to make use of the ADC's full dynamic range.

The antenna was designed to provide a gain of 15 dBi, which is sufficient to provide reasonably high baseband voltages. A planar patch array similar to that shown in [7] was developed and designed to be compact and lightweight while still providing sufficient gain. Its radiation diagram, which focuses the beam in the vertical plane but shows a relatively wide beam in the horizontal plane, facilitates system alignment.

Hardware Demonstrator

The system design aspects as previously described were applied to the fabrication of the hardware demonstrator

depicted in Figure 4. An operating frequency of 24 GHz was chosen because a device operating at that frequency can use commercially available components and still be within an acceptable weight and size range. The silicon-germanium BGT24LTR11 MMIC from Infineon Technologies was used for the radar transceiver because it contains a suitable VCO tailored for the frequency band of interest. The MMIC also uses a 1:16 frequency divider, an LNA, and a quadrature homodyne downconversion mixer in a small package measuring 2.7×2.7 mm^2. The VCO is stabilized using the ADF4112 integer-N PLL from Analog Devices and a TCXO that serves as a phase reference. In the baseband section, noninverting operational amplifiers are used, and the digitization is accomplished by the ADC of the STM32L4 microcontroller from STMicroelectronics. The data are sent via a universal asynchronous receiver transmitter (UART) first to a chip from Future Technology Devices International along with a custom-made, low-weight universal serial bus connector (presented in [7]) and then to the laptop where the data are processed.

No traces were routed on the inner signal layer below the top layer so that the ground plane for the digital and RF signals could provide low impedance. This ensured that noise was a low as possible for the entire layout, adding several low-dropout regulators and ferrite beads for the different voltage supplies suppresses noise on these traces and thus improves the system's noise performance as well as the precision of the ADC.

Using a four-layer rather than a two-layer PCB stack contributes to saving space. The bottom layer can be used for traces and components. As a result, the entire demonstrator weighs under than 12 g. Rogers RO4350B laminates were used as the RF substrates on the top and bottom layer. These low-cost laminates are tailored for frequencies higher than 24 GHz.

Measurements

Measurement Noise

To verify the functionality of the proposed system prototype, different measurements were taken and compared to the simulations. First, the phase-noise spectrum of the system was recorded using a Rohde & Schwarz signal source analyzer. As can be seen in Figure 5, a low phase noise of –78 dBc/Hz could be measured at an offset frequency of 10 kHz from the carrier, which nearly matches the noise from the simulation (–82 dBc/Hz). Because it depends on the baseband bandwidth, the rms error contribution to distance measurements caused by phase noise can be calculated. This was calculated for both the simulated and measured phase noise (Figure 6), where the differences in both curves at low bandwidths are caused by imperfect modeling of the TCXO's phase noise and, in particular, the absence of flicker noise in the simulations. In addition, the rms range error contribution due to phase noise is well below the required system sensitivity of 10 μm for the chosen effective bandwidth of 10 kHz. Even though higher bandwidths were possible from the perspective of phase noise, other noise contributions, such as amplifier noise, would then strongly affect the measurement.

Displacement Measurement

In the next step, the system was set up according to the competition scenario as described previously. Figure 7 shows the measured displacement of a metal plate moving sinusoidally with a peak-to-peak amplitude of

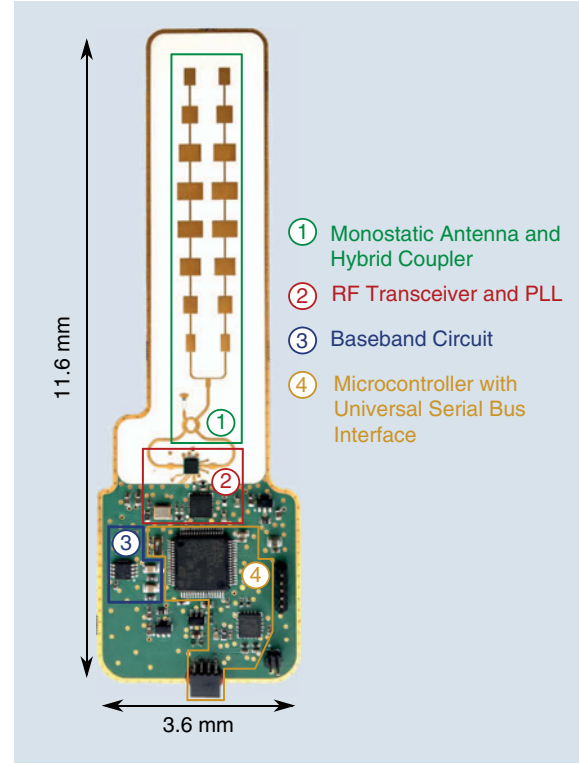

Figure 4. *The fabricated radar PCB.*

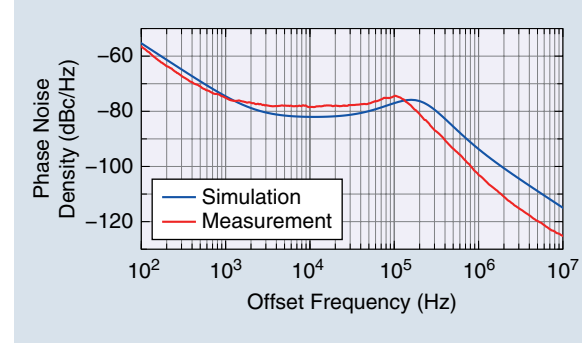

Figure 5. *Simulated and measured closed-loop oscillator phase noise.*

The antenna was designed to provide a gain of 15 dBi, which is sufficient to provide reasonably high baseband voltages.

10 μm at a distance of 1 m. The comparison with the actual displacement of the metal plate clearly confirms the functionality of the system for even very small displacements. Note that the frequency of the oscillation (0.4 Hz) could be estimated correctly in fewer than 5 s using a Fourier transform.

Energy Consumption and Pulse Timing

As discussed previously, minimal energy consumption was not the primary optimization parameter of the system. However, to maximize the achieved score, the power consumption had to be decreased as well. This was achieved by precisely switching and reducing the duty cycles of the active components. Performing only ten measurements per second, the active components are powered off most of the time.

The current consumption during one measurement with the different power-on and power-off periods is shown in Figure 8. At time ①, the microcontroller's "wake up" is triggered by an internal timer interrupt. Prior to this, it remains in a sleep mode that is as deep as possible and switches to "awake" as necessary without requiring that its peripherals reset. The microcontroller's wake up is triggered by an internal timer interrupt. After booting, the TCXO is enabled at time ②. A few hundred microseconds later, the PLL and the VCO are powered-on at ③. Because the baseband bandwidth is rather narrow to reduce the noise in the downconverted signals, the PLL and VCO must remain on for a longer time. As a consequence, the I and Q signals are digitized immediately before time ④, when the RF part of the system is disabled again. After the data have been sent using the UART interface, the microcontroller enters its sleep mode again at event ⑤.

By integrating current consumption, which consists of ten single equally spaced measurements over 1 s, as shown in Figure 8, the overall power consumption can be calculated. The average current, which is drawn over 1 s, can thus be determined as 0.75 mA, resulting in a power consumption of 2.5 mW when multiplied with the supply voltage of 3.3 V.

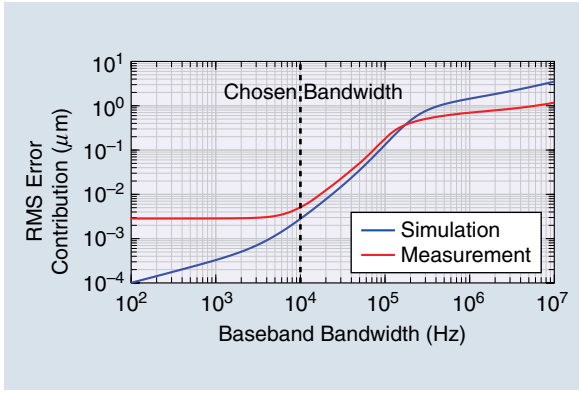

Figure 6. *The calculated contribution of simulated and measured phase noise to the precision of the displacement measurements at a distance of 1 m.*

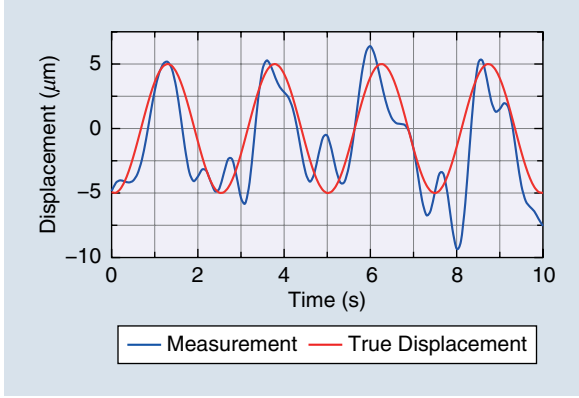

Figure 7. *The displacement measurement of a target oscillating with a peak-to-peak amplitude of 10 μm at a frequency of 0.4 Hz.*

Comparison to Previous Work and Conclusion

We show here that it is possible to design a high-performance, short-range radar system that is lightweight and compact. This was made possible by a careful choice of circuit components and a suitable design of the RF and baseband circuitry. Dedicated firmware was developed to control all system components and introduce a duty cycle for an energy-saving pulsed operation mode. Moreover, improved signal processing of the acquired data decreased the system's response time to fewer than 5 s for all amplitudes.

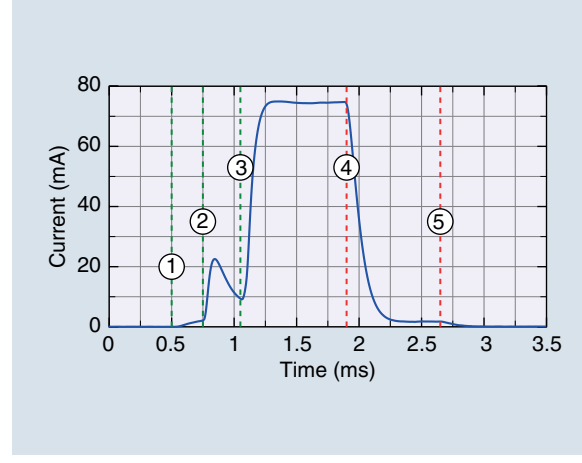

Figure 8. *The current consumption during a single pulse.*

TABLE 3. A comparison of the proposed system with designs from previous years' SDCs.

	Sensitivity	Weight	Response Time	Power Consumption	Estimated Component Costs
SDC2014 [11]	500 μm	5 g	<60 s	1.5 mW	US$176
SDC2015 [12]	100 μm	123 g	14 s	1115 mW	>US$47
SDC2017 [7]	100 μm	7.9 g	8.9 s	0.03 mW	US$99
This work	10 μm	11 g	<5 s	2.5 mW	US$33

A feature of the system not factored into the competition's FOM is that it was built using only commercial, off-the-shelf components, which are easy to obtain and often inexpensive. The costs of the major components—not including the surface-mount resistors, capacitors, and PCB fabrication—is as low as US$33 with this design. When possible mass production and price reductions by distributors are taken into account, the cost drops to only US$19. The price for a single prototype has also been estimated for the designs from previous years' competitions in Table 3, using recent prices obtained by the authors. All previous designs were considerably more expensive.

Each year, the scenario and the FOM for the student competition are changed somewhat to encourage participants to come up with new ideas and be adaptable. In 2014, the minimum amplitude to be detected was 500 μm. The winning design [11] was based on a homodyne receiver with a variable reflect or to switch the phase of the reference signal. An audio port of a personal computer was used for digitizing the alternating I and Q signals. Consequently, only a small PCB and very few components were needed, making it the lightest system so far.

However, it was not suitable for the next competition in 2015, where the minimum amplitude to be detected was lowered to only 10 μm. That year, the winning team [12] used mixer MMICs for the downconversion of the Doppler signals at 5.8 GHz. With this approach, small amplitudes of up to 100 μm could still be detected.

To compete with this design, an ultralow-power system making use of a six-port receiver at 24 GHz was presented in 2017 [7]. Even though it set a record for power consumption of only 30 μW on average, it was not suitable for the 2018 competition because the focus was shifted from low power to high sensitivity by an adjustment of the FOM. At the expense of a slight increase in power consumption and overall weight, target displacement amplitudes of 10 μm could be detected for the first time by the design presented here.

With continuous advances in microwave engineering leading to higher integration densities and better performance of the devices on the one hand [13] and good progress in the field of signal processing on the other, ongoing improvement in designs for future SDCs will lead to exciting competitions in coming years.

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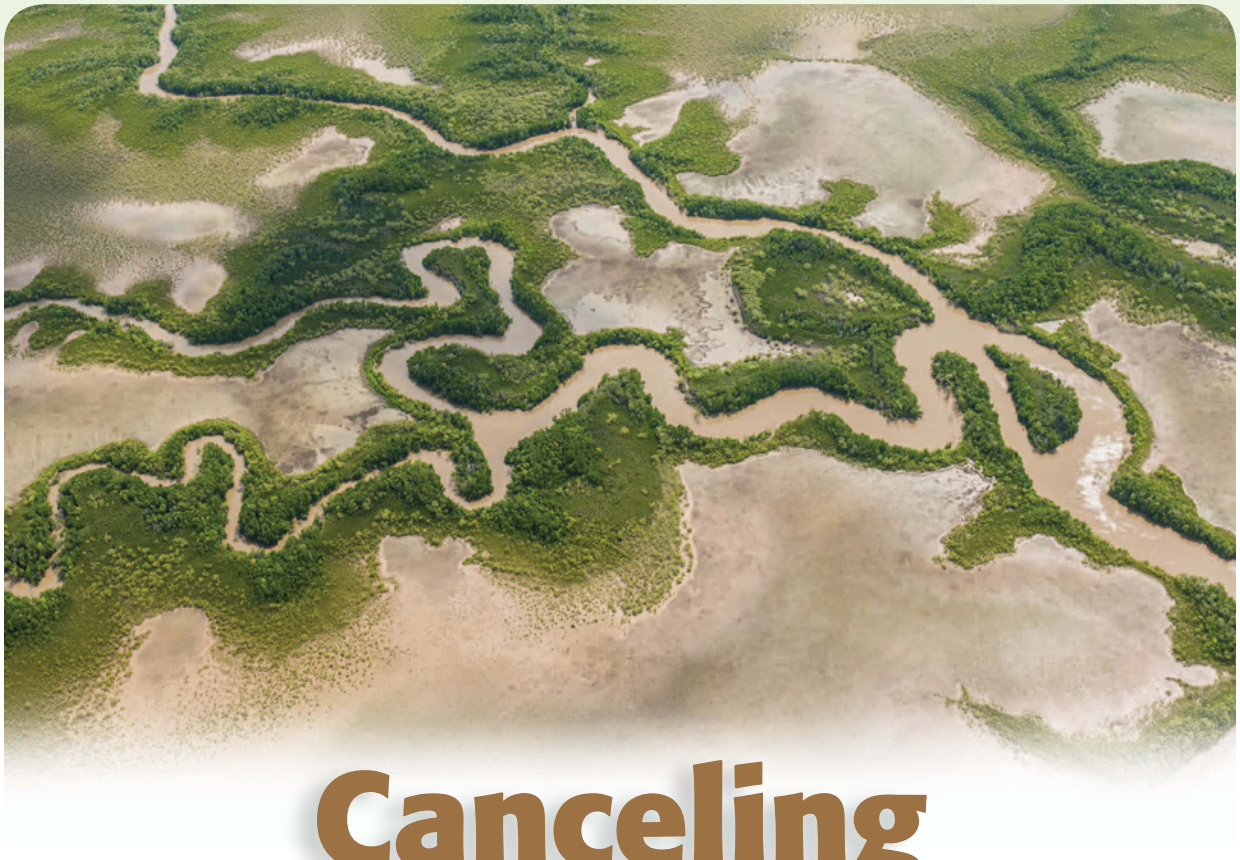
2018 Student Design Competition Winners IMS

High-Efficiency Power Amplifier



Canceling Intermodulation Products

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During the 2018 IEEE Microwave Theory and Techniques Society (MTT-S) International Microwave Symposium (IMS2018) in Philadelphia, Pennsylvania, the Student Design Competition (SDC) for a high-efficiency power amplifier (PA), sponsored by the MTT-S Technical Committee on Microwave High-Power Techniques, celebrated its 14th anniversary. This competition aims to challenge the maximum power-added efficiency (PAE) of PAs without compromising linearity performance.

Rules and Strategies

Suit the strategy to the mission! For electronic engineering, analyzing the specifications to be satisfied is the primary preparatory work. The rules of the competition can be summarized as follows.

1) *Output power and operating frequency*: When excited by a single carrier, the PA must produce an output power between 4 and 40 W at an operating frequency (f_0) between 1 and 10 GHz.
2) *Continuous wave (CW) and dc supplies*: The PA should require a maximum of two dc supplies for operation and fewer than 24 dBm of input power to reach the minimum 4-W output power when excited using a CW single carrier at f_0.
3) *Two-tone signal linearity and PAE*: Linearity measurements are conducted using two equal-amplitude carriers spaced 5 MHz apart (f_0 centered), with a maximum of 21-dBm input power per tone. The $\mathrm{PAE}_{@C/I=30}$ is obtained when the PA is producing a two-tone carrier-to-intermodulation (C/I) ratio of 30 dB.
4) *The final figure of merit (FOM)*: The FOM used to evaluate the PAs is defined as

$$\mathrm{FOM} = \mathrm{PAE}_{@C/I=30} * (f_0)^{0.25}. \tag{1}$$

5) The winner will be the PA that achieves the highest FOM.

The output power requirement and operating frequency range in rule 1 make high-electron mobility transistors (HEMTs) a better choice for the transistor. Rule 2 makes it unwise to use complicated structures that need too many dc supplies, due to the dc–dc loss involved. Rule 3 demands that the design balance two conflicting specifications, linearity and efficiency. From rule 4, the operating frequency also weights the FOM. These rules make the class-AB PA and Doherty PA (DPA) the most promising solutions.

For class-AB operation, choosing an appropriate gate bias can allow the second-order sweet spot to create a large C/I over a wide power range. So, while class A is usually regarded as the most linear mode of operation, by taking advantage of the double sweet spot, class AB may be more linear over a wide power range, and a better efficiency can be achieved, making the class AB the better choice for the design of a single-way linear PA [2].

The Doherty structure using active load modulation (LM) is also considered one of the most promising design methods for this SDC [3], because of its simple structure, efficient operation over a large output power range, and linear potential introduced by the cancellation between the carrier and peaking transistors [4].

Theory and Design

The linearity analysis of the DPA is more complicated than that of a conventional class-AB amplifier. For a DPA, the carrier PA is biased at class AB, and the peaking PA is biased at class C to realize the active LM in a large output power range.

Theory of the Linear DPA

The ideal operation diagram of a DPA is shown in Figure 1. The impedances and currents of the carrier and peaking PAs can be calculated as

$$\begin{cases} I_C' = \dfrac{Z_C I_C}{Z_T} = I_C Z_T - I_P \\ I_L = I_C' + I_P = I_C Z_T \end{cases}. \tag{2}$$

As shown in (2), the linearity of DPAs is determined by the carrier PA because the contribution of a peaking PA does not act directly on the output power but rather via the active LM. However, in practice, the output power of the peaking PA can also be transferred from the nonideal components directly into the load; thus, the linearity of the DPA could be enhanced [3].

The linearity of the amplifier is determined solely by the carrier amplifier at low power levels due to the shutting down of the peaking PA. Therefore, the carrier amplifier is always biased at class AB to achieve better linearity and efficiency. When the DPA reaches high power levels, appropriate phase shifting and amplitude adjustment can improve the entire linearity of the amplifier, utilizing the harmonic and intermodulation product cancellation between the carrier PA and the peaking PA [3], [5]. Therefore, the DPA is capable of operating linearly and more efficiently than for conventional class-AB operation PAs [4].

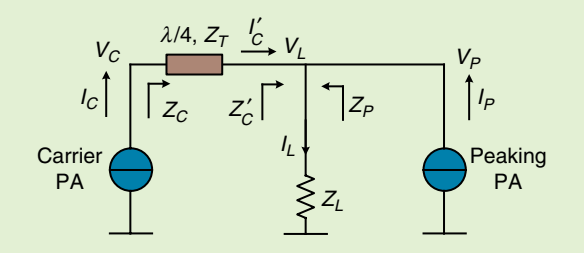

Figure 1. *An operational diagram of the DPA.*

Comparable performance, along with the fixed 50-Ω impedance isolation resistor and microstrips, makes it possible to provide a stable and easily realized topology for subtle tuning of the power-splitting ratio and helps to simplify the final optimization of the printed circuit board.

However, the entire power gain of the DPA suffers from gain compression at the lower input power level due to the class-C operation of the peaking PA and the power division of the input power, especially with the conventional symmetric DPA. When driven by two-tone signals, there will be two causes of deterioration of C/I over the whole power range. The first deterioration occurs when the class-C biased peaking PA is opening. With the increase in input power, the gain expansion from the peaking PA will impact the overall power gain and thus lead to the second deterioration of C/I.

Considering the characteristics of the HEMT transistor, intermodulation products of greater than the fifth order can be neglected. To guarantee a C/I under the level of 30 dB, the third- and fifth-order intermodulation (IMD3 and IMD5) bulges caused by the deterioration of C/I must be well controlled. The IMD3 can be improved by adjusting the specific bias condition with a small quiescent current. However, tuning the quiescent operating point of the DPA not only affects IMD3 but also impacts IMD5. In fact, IMD5 becomes worse when IMD3 is improved.

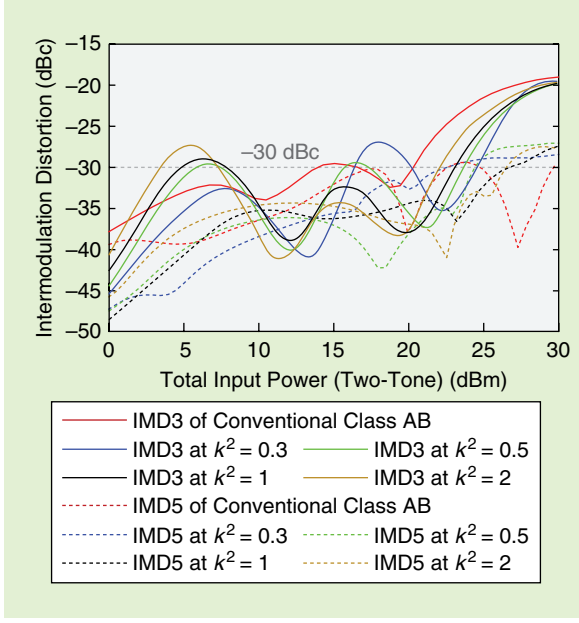

Figure 2. *The simulated IMD3 and IMD5 of the class-AB PA and DPA with varying power-splitting ratios.*

An additional controllable factor generated from the asymmetric structure of some DPAs could provide further possibilities for IMD3 and IMD5 cancellation between the carrier PA and the peaking PA; we provide closer analysis in the next section.

Linear Improvement of Asymmetric DPA

An asymmetric DPA structure potentially provides more flexibility for linearity improvement while maintaining PAE. There are three methods to realize an asymmetric DPA: asymmetric transistors, different drain voltages, and unequal power division. Currently, only a handful of unmatched commercial transistors can meet rule 1 while maintaining a highly precise model. Furthermore, transistors with large differences of power capability in a DPA will directly influence the entire PAE; thus, there are not many options to choose from. Additionally, due to the restriction of rule 2, generating an extra drain voltage or the negative gate voltages from the positive large drain voltage will introduce unbearable dc–dc converter loss, which may lead to an efficiency reduction of 2–10%.

Hence, the best possible solution is to implement an asymmetric DPA using an unequal power-splitting ratio. By applying more power to the carrier PA via an unequal power divider, the output power of the carrier PA will increase, and so the C/I fluctuation caused by the opening of the peaking PA can be weakened. Moreover, clipping from the gain compression at the low power level can also be diminished.

For a given load impedance and quiescent operating point, the input voltage v_{gs} is regarded as the only factor that determines drain current i_{DS}. By introducing transconductance coefficients, then normalizing by means of the maximum carrier $I_{max,C}$ and peaking drain current $I_{max,P}$, i_{DS} can be simply expressed using the Taylor series:

$$\begin{cases} i_{DS,C} \approx I_{DS,C} + I_{max,C}(g_{m1,C}v_{gs} + g_{m2,C}v_{gs}^2 \\ \qquad + g_{m3,C}v_{gs}^3 + g_{m4,C}v_{gs}^4 + g_{m5,C}v_{gs}^5) \\ i_{DS,P} \approx I_{DS,P} + I_{max,P}(g_{m1,P}v_{gs} + g_{m2,P}v_{gs}^2, \\ \qquad + g_{m3,P}v_{gs}^3 + g_{m4,P}v_{gs}^4 + g_{m5,P}v_{gs}^5) \end{cases} \tag{3}$$

where $I_{DS,C}$ and $I_{DS,P}$ are the quiescent drain currents and $g_{m1,C} \sim g_{m5,C}$ and $g_{m1,P} \sim g_{m5,P}$ are the normalized transconductance coefficients for the carrier and peaking PAs, respectively, at each given quiescent operating point.

To explain this phenomenon, suppose the two-tone input signal v_{gs} can be expressed as

$$v_{gs} = A(\cos w_1 t + \cos w_2 t), \tag{4}$$

where A is the amplitude of each tone ($A \geq 0$) and w_1 and w_2 are the frequencies of the two-tone signal.

Assume that the power-splitting ratio of the input power divider is defined as

$$k^2 = \frac{P_{\text{peak}}}{P_{\text{main}}}. \tag{5}$$

After power division and a phase shift of φ, according to (4), the amplitude-normalized signal delivered to the carrier and peaking PAs can be written as

$$\begin{cases} v_{\text{gs},C} = \cos w_1 t + \cos w_2 t \\ v_{\text{gs},P} = k(\cos(w_1 t + \varphi) + \cos(w_2 t + \varphi)) \end{cases}. \tag{6}$$

By substituting (6) into (3) and considering fifth-order products, the coefficients of the normalized expanded IMD3 and IMD5 of the carrier and peaking PAs can be written as

$$\begin{cases} I_{\text{IMD3},C} = \frac{3}{4} g_{m3,P} \cos(\text{IMP}_3) + \frac{25}{8} g_{m5,P} \cos(\text{IMP}_5) \\ I_{\text{IMD3},P} = \frac{3}{4} g_{m3,C} k^3 \cos(\text{IMP}_3 + \varphi) \\ \qquad\qquad + \frac{25}{8} g_{m5,C} k^5 \cos(\text{IMP}_5 + \varphi) \\ I_{\text{IMD5},C} = \frac{5}{8} g_{m5,C} \cos(\text{IMP}_5) \\ I_{\text{IMD5},P} = \frac{5}{8} g_{m5,P} k^5 \cos(\text{IMP}_5 + \varphi) \end{cases}, \tag{7}$$

where IMP_3 and IMP_5 are the IMD3 and IMD5 products, respectively. From the formulas in (7), at the given quiescent operating point, the extra factor k in IMD3,P and IMD5,P makes the asymmetric DPA more flexible than the symmetric DPA for meeting the phase and amplitude requirements of IMD3 and IMD5 cancellation between the carrier and the peaking PAs. Thus, more efficient and linear performance can be achieved.

For comparison, the simulated IMD3 and IMD5 of the class-AB PA and DPA with varying k^2 are shown in Figure 2. These results are achieved under the condition of ideal conventional matching and biasing. When $k^2 = 1$, the DPA is operating symmetrically. The extra factor k in the asymmetric DPA provides a larger space for the control of IMD3 and IMD5 than the symmetric DPA and class-AB PA can provide.

Accurate Power Division for the Asymmetric DPA

The optimized power-splitting ratio of the asymmetric DPA always needs subtle tuning. However, the nonfixed isolation resistor values and the varying width of microstrip lines are hard to satisfy perfectly.

To obtain optimized performance, a flexible topology consisting of an unequal power divider using uniform 50-Ω microstrip lines and a fixed 50-Ω isolation resistor is applied; the topology is available for any power-splitting ratio. The detailed theory is well analyzed in [6], a previous work by some members of

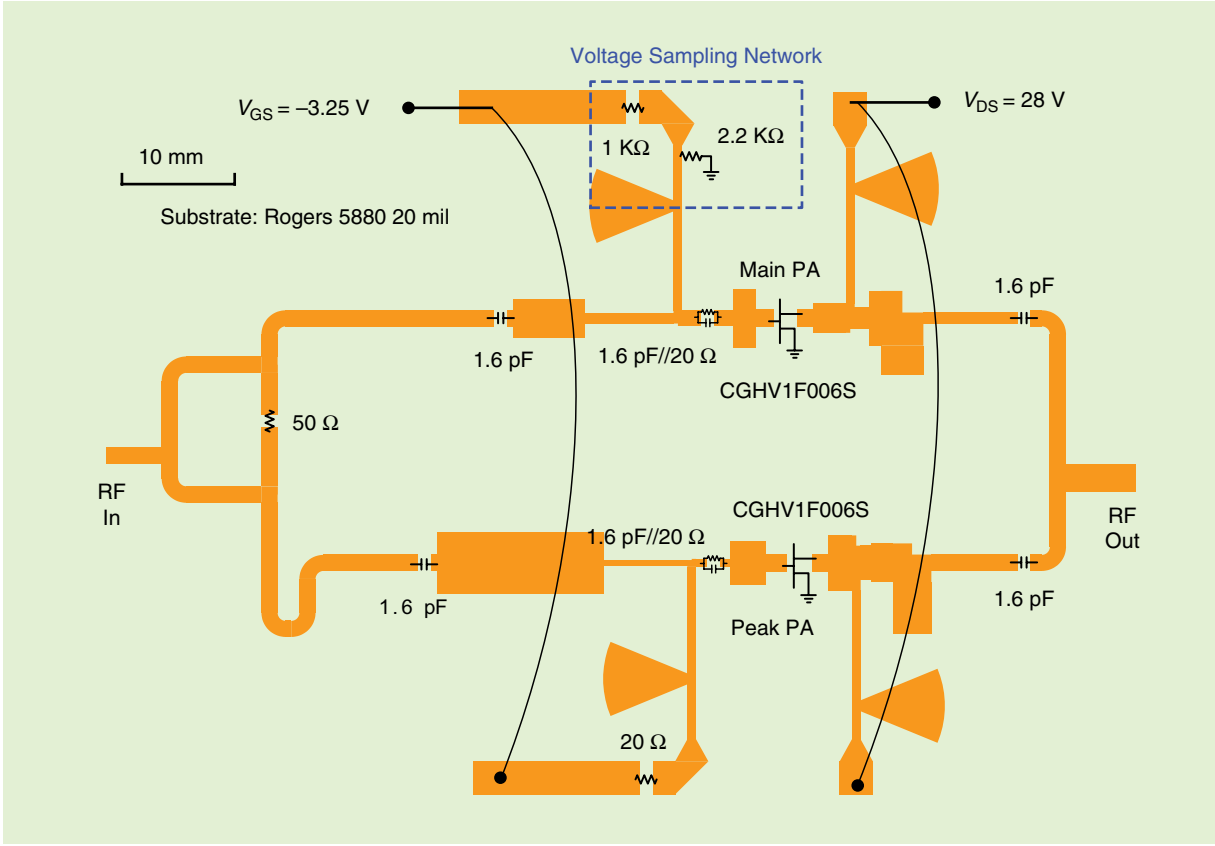

Figure 3. *The topology of the designed DPA for the IMS2018 SDC for a high-efficiency PA.*

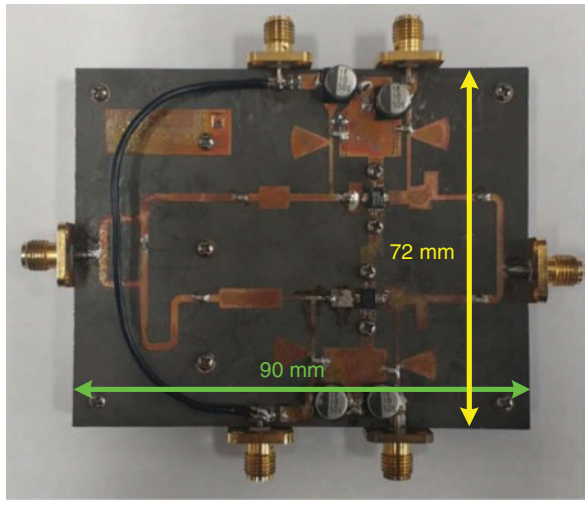

Figure 4. *The designed DPA for the SDC.*

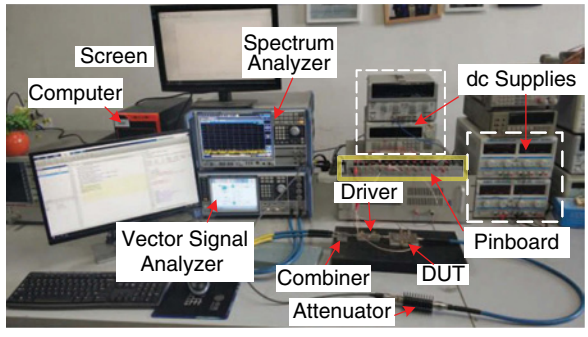

Figure 5. *The measurement environment.*

this article's author team. Comparable performance, along with the fixed 50-Ω impedance isolation resistor and microstrips, makes it possible to provide a stable and easily realized topology for subtle tuning of the power-splitting ratio and helps to simplify the final optimization of the printed circuit board (PCB). Note that the k^2 of the power divider introduced in this work is designed to be 0.6 at 5.35 GHz.

Stability Enhancement and Memory Effects Reduction

For both the carrier and peaking PAs, RF thin-film resistors are introduced in the gate bias and input networks to enhance the stability of the DPA. Electrolytic capacitors and multilayer ceramic capacitors are applied in all bias networks to suit the envelope impedance, which weakens the IMD3 or IMD5 asymmetry caused by the electrical memory effect.

Manufacturing and Fabrication

Considering the operating frequency weight in the FOM, a 250-nm gallium-nitride HEMT Cree CGHV1J006S is introduced to design the linear and efficient DPA at 5.35 GHz, and a weight of 1.52 ($5.35^{0.25}$) is obtained. The circuit

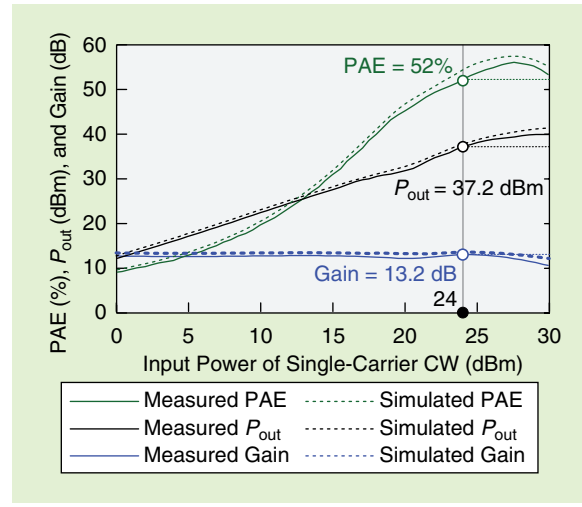

Figure 6. *The measured and simulated PAE, P_{out}, and gain of the designed DPA versus the CW input signal.*

was fabricated using a low-loss Rogers substrate 5880 ($\varepsilon_r = 2.2$, $h = 20$ mil, $\tan\delta = 0.0004$) and high-accuracy components to reduce errors in the manufacturing process. A 10-mm-thick duralumin heat sink is tightly screwed together with the PCB to ensure that the PCB is well grounded; this also helps dissipate heat from the transistors. The topology and a photograph of the designed DPA for the IMS2018 SDC for a high-efficiency PA are shown in Figures 3 and 4, respectively.

Measurement Setup and Results

The measurement environment is shown in Figure 5. A Rohde & Schwarz two-way vector signal generator SMW200A is used to generate the CW and two-tone signal. The 5-MHz spaced, two-tone signal is generated separately and added by a combiner, then preamplified by the driver to drive the device under test (DUT). Attenuated using a −40-dB attenuator and after a series of calibrations, the output performance of the DUT was measured by the Rohde & Schwarz frequency and spectrum analyzer.

To satisfy rule 2 of the competition, two dc sources were used to supply the DUT: a positive-voltage 28 V and a negative-voltage −3.25 V. The positive voltage is simply split into two parts, one for the drain voltages of the main PA and one for the peaking PA. The negative voltage is used to bias the peaking PA at a slight class C; by applying the voltage-sampling network, another negative voltage −2.23 V is obtained to bias the main PA at class AB to achieve a better low power linearity. (See Figure 2; thanks to the imperceptible gate current, the voltage-sampling network produces little power consumption.) These dc supplies guarantee a quiescent operating point with a total 80-mA drain current: all of the measurement results in this article were obtained at this quiescent operating point.

Note that the DPA is designed at 5.35 GHz. However, due to some fabricaton errors and welding losses,

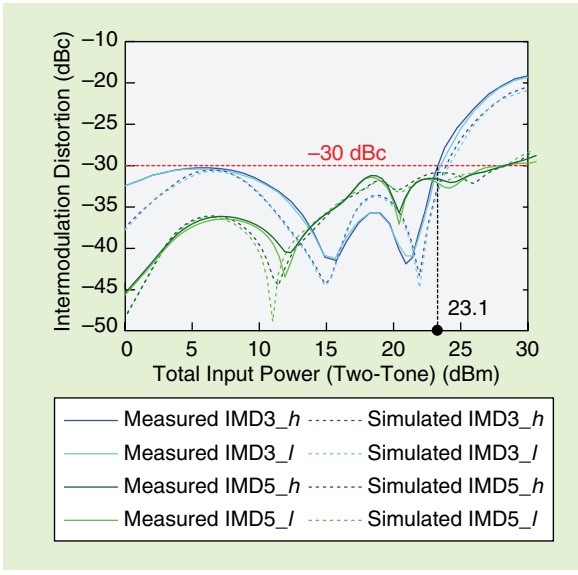

Figure 7. *The measured and simulated IMD3 and IMD5 of the designed DPA versus total input power of a 5-MHz spaced, two-tone signal at 5.337 and 5.342 GHz.*

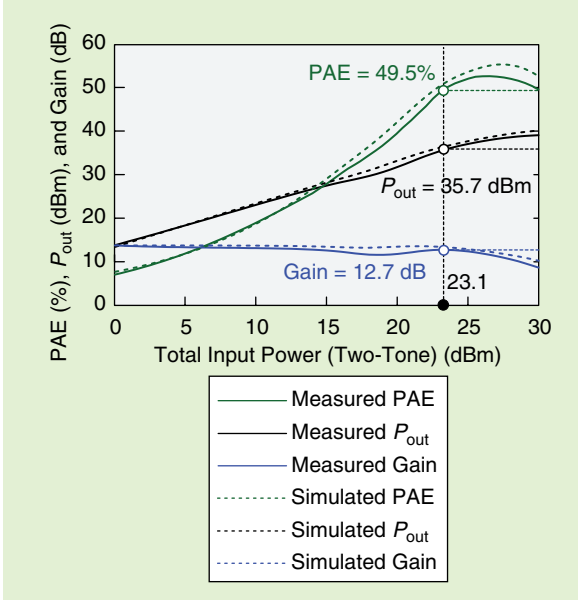

Figure 8. *The measured and simulated PAE, P_{out}, and gain of the designed DPA versus total input power.*

the optimized performance is observed at the center frequency of 5.3395 GHz.

First, to meet the requirement of output power in rule 2, the DPA is tested using a single-carrier CW signal at 5.3395 GHz. The measured PAE, output power P_{out}, and gain versus the input power of the CW signal are shown in Figure 6. The output power reaches 37.2 dBm with 52% PAE when driven using 24-dBm input power.

Frequencies 5.337 and 5.342 GHz were selected for the 5-MHz spaced, two-tone test. The IMD3 and IMD5 versus total input power are plotted in Figure 7. The C/I = 30 dB specification is reached when the total two-tone input power reaches 23.1 dBm (20.1 dBm per tone). The measured PAE, P_{out}, and gain versus total input power are shown in Figure 8. The corresponding 35.7-dBm P_{out} and 49.5% PAE are achieved when driven by 23.1-dBm total two-tone input power. Figures 6–8 indicate good agreement between measurements and simulation results.

Finally, based on the single CW (5.3395 GHz) P_{out} of 37.2 dBm at 24-dBm input power and the corresponding two-tone (5.337 and 5.342 GHz) PAE of 49.5% when the first C/I = 30 dB is observed, according to the rules, an FOM of 75.2 is obtained.

Conclusions

This article presented the design and validation of the winning entry in the IMS2018 SDC for a high-efficiency PA. The design applies an asymmetric DPA with unequal power division to achieve cancellation of both IMD3 and IMD5 between the carrier and peaking PAs. Experimental testing demonstrated good overall agreement between the simulation and measurement, which verified the design method. The designed DPA exhibits both high efficiency and good linearity. The measured performance is 49.5% two-tone PAE at −30 dBc IMD3, obtaining the FOM of 75.2.

Acknowledgments

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2018 Student Design Competition Winners IMS

Reconfigurable Bandpass Filter

Suppressing In-Band Interference

FOOTAGE FIRM, INC.

Dakotah J. Simpson, Andrea Ashley, and Dimitra Psychogiou

Because of today's exceedingly crowded radio spectrum, in which multiple sources of dynamic interference can desensitize a radio's receiver, the design of bandpass filters (BPFs) with adjustable transfer function characteristics has become a critical topic of research [1]–[14]. Out-of-band interference has been traditionally addressed by increasing the filter order, but the suppression of in-band interfering signals requires more sophisticated preselect RF filtering solutions, particularly for dynamic jamming scenarios. These include the integration of tunable bandstop filters (BSFs) in front of the preselected BPF [2]–[4] or the realization of BPFs with in-band interference suppression capabilities through incorporated BPF/BSF

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architectures that are codesigned to miniaturize the size of the preselected RF front-end stage [5]–[11].

To address these challenges, the reconfigurable bandpass filter Student Design Competition (SDC) of the 2018 IEEE Microwave Theory and Techniques Society International Microwave Symposium (IMS 2018) held in Philadelphia, Pennsylvania, focused on the realization of compact RF filtering solutions for in-band interference suppression in the L-band due to the increasing number of coexisting applications in this spectrum. In this article, we present the work that was granted the first-place award in this category and describe the RF design and practical development of a lumped-element (LE)–based BPF with a continuously tunable in-band rejection band. The proposed filter concept is based on a static, wideband BPF architecture in which a frequency-tunable in-band notch is introduced by incorporating BSF sections into the BPF's resonators.

Competition Objectives

The main objectives of the SDC were the RF design and implementation of a compact BPF centered at 1.2 GHz that is capable of performing three different scenarios:

- reject an interfering signal located in the middle of the passband (i.e., at 1.2 GHz), while retaining minimum insertion loss (or noise figure) from 1.1 to 1.15 GHz and 1.25 to 1.3 GHz and maximum rejection from 1.175 to 1.225 GHz
- reject an interfering signal above the passband (i.e., at 1.4 GHz), while retaining minimum insertion loss (or noise figure) from 1.1 to 1.3 GHz and maximum rejection at 1.4 GHz
- reject an interfering signal below the passband (i.e., at 1.0 GHz), while retaining minimum insertion loss (or noise figure) from 1.1 to 1.3 GHz and maximum rejection at 1.0 GHz.

A conceptual illustration of these interference suppression scenarios is shown in Figure 1. The filter design was left open to the competing teams, and any electronic components and substrate materials could be used, including but not limited to active devices, varactor diodes, switches, and LEs. For passive filter entries, the passband metric was insertion loss; for active filter entries, the passband metric was noise figure. In addition, the designed filter area needed to be as small as possible.

Filter Design

Proposed Concept: Wide-Band BPF with In-Band Interference Suppression

A variety of approaches could have been used to meet the specifications of the SDC. These include a series-cascaded tunable BSF and a static BPF, examples of which are presented in [2]–[4]. However, this solution leads to fairly large form factors due to the use of two distinct filters and is mostly suited for out-of-band interference suppression because of the mismatch between the two filtering stages if the BSF is placed within the BPF passband. In an alternative configuration, a filter with switchable static notches could also have been used

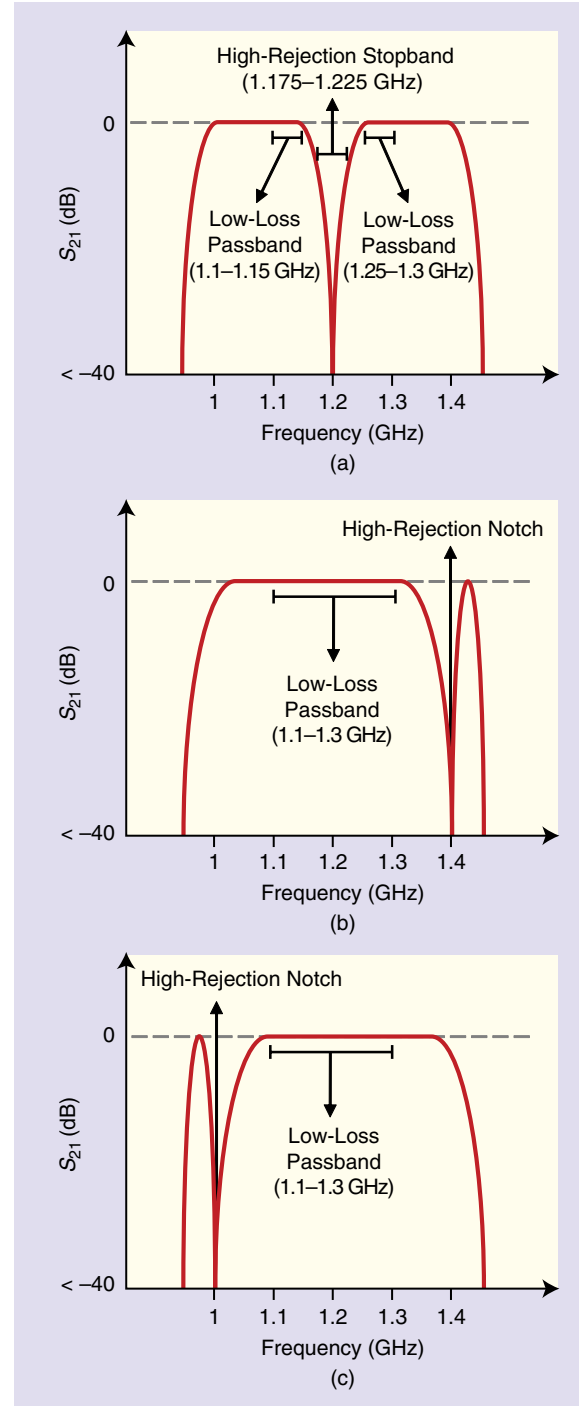

Figure 1. *A conceptual illustration of the expected filtering transfer functions of the bandpass filter with in-band interference suppression capabilities under various interference scenarios: (a) 1.2-GHz scenario, (b) 1.4-GHz scenario, and (c) 1.0-GHz scenario.*

[5], [6]. However, RF switches may result in increased levels of insertion loss; therefore, based on the given interference scenarios, three individual structures (i.e., one for each frequency of interference) would have been needed, thus increasing the overall filter size.

Based on the competition objectives and the size and RF performance limitations of these approaches, we designed, manufactured, and measured a wideband BPF with a continuously tunable in-band notch. Our proposed filter design was based on a static, wide-band BPF architecture in which a frequency-tunable in-band notch is embedded by incorporating BSF sections into the BPF's resonators [10], [11]. The BSF sections are frequency-tunable, series-type resonators that introduce a frequency-reconfigurable transmission zero (i.e., the in-band notch). By embedding the BSF sections into the BPF's resonators, we could significantly reduce the number of filter elements when compared with a conventional series-cascaded filter design [2]–[4].

Because the physical area of the filter was a significant factor in the competition evaluation, we focused on an RF architecture with small physical size. To achieve this goal, we concentrated on 1) an RF codesigned BPF/BSF scheme and 2) a practical realization scheme using surface-mounted devices.

Theoretical Foundations of the BPF Concept with In-Band Interference Suppression

The coupling routing diagram of the proposed second-order BPF with an embedded tunable in-band notch is shown in Figure 2(a). It is based on the filter concept in [10] and [11], which we tailored to the competition needs. The circuit consisted of a static BPF section, made up of two static resonating nodes and three impedance inverters (which give rise to the overall bandpass response), and two frequency-tunable BSF sections. The sections were shaped by two impedance inverters and two frequency-reconfigurable resonating nodes that create the tunable in-band notch. The normalized coupling matrix of the proposed filter is as follows:

$$[M] = \begin{bmatrix} 0 & M_{12} & 0 & 0 & 0 & 0 \\ M_{12} & M_{22} & M_{23} & M_{24} & 0 & 0 \\ 0 & M_{23} & M_{33} & 0 & 0 & 0 \\ 0 & M_{24} & 0 & M_{44} & M_{45} & M_{46} \\ 0 & 0 & 0 & M_{45} & M_{55} & 0 \\ 0 & 0 & 0 & M_{46} & 0 & 0 \end{bmatrix} = \begin{bmatrix} 0 & 0.78 & 0 & 0 & 0 & 0 \\ 0.78 & 0 & 0.32 & 0.64 & 0 & 0 \\ 0 & 0.32 & M_{33} & 0 & 0 & 0 \\ 0 & 0.64 & 0 & 0 & 0.32 & 0.78 \\ 0 & 0 & 0 & 0.32 & M_{55} & 0 \\ 0 & 0 & 0 & 0.78 & 0 & 0 \end{bmatrix}, \quad (1)$$

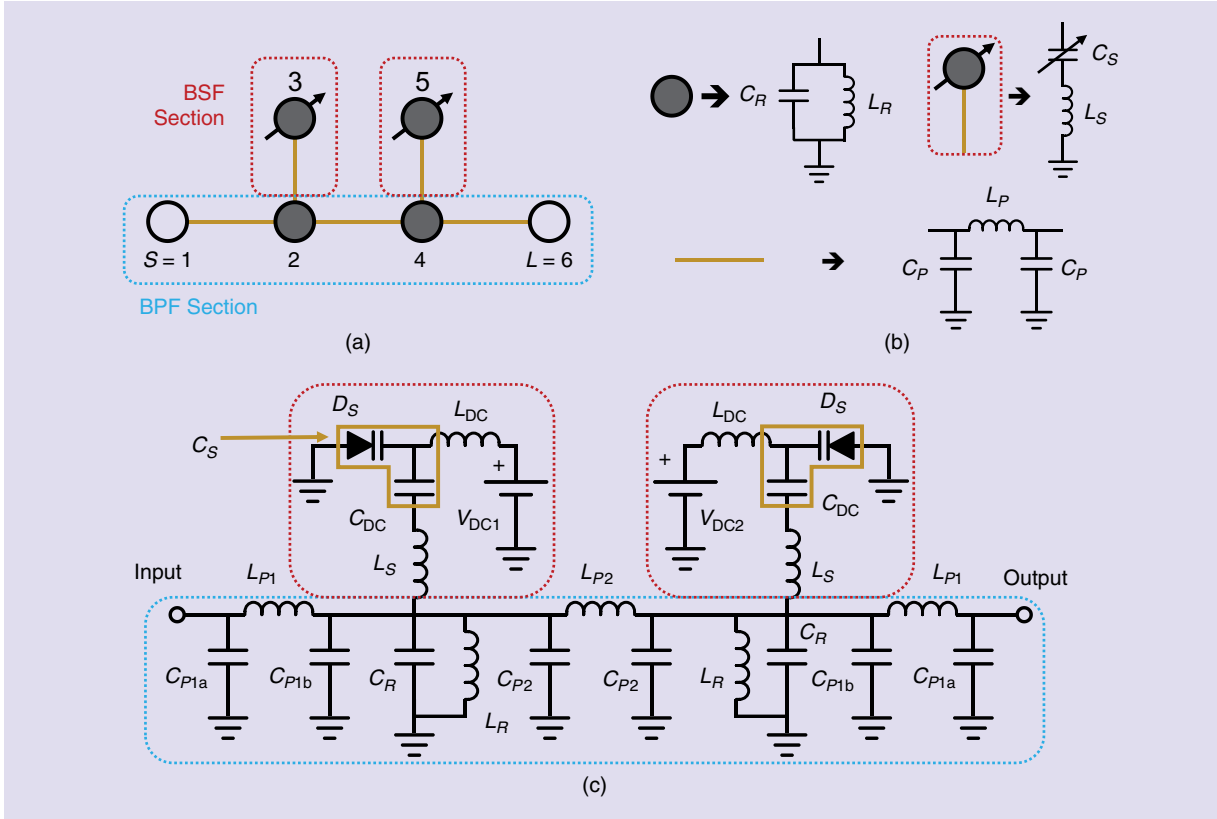

Figure 2. *(a) The coupling routing diagram of the proposed second-order bandpass filter with tunable in-band notch. The black circles indicate resonating nodes, white circles indicate source and load, and solid lines indicate coupling elements. (b) The LE realizations of the coupling routing diagram segments. (c) An overall circuit schematic of the filter.*

where the diagonal elements represent the self-coupling coefficients of the resonators (i.e., their normalized frequency offsets), and all other values represent the normalized internode coupling coefficients between resonating nodes [11], [15].

In the design, the self-coupling coefficients of the BPF resonators are set to zero, and the BPF center frequency is set to 1.2 GHz when a lowpass-to-bandpass frequency transformation centered at 1.2 GHz is used. The coefficients of the BSF resonators are left as variables so that the center frequency of the notch can be assigned to the desired location.

To verify that the coupling matrix provides the desired response, multiple power transmission and reflection responses were synthesized using conventional filter synthesis (Figure 3). In particular, Figure 3(a)–(c) shows the notch located at the interfering frequencies, f_{BS}, specified in the competition objectives (1.2 GHz, 1.4 GHz, and 1.0 GHz, respectively). In an LE-based integration scheme, the resonators have a limited unloaded quality factor (Q_U), and these figures show a comparison between a filter that has ideal resonators and one that has lossy resonators with $Q_U = 100$. When lossy resonators are used, the notch rejection is approximately 40 dB. Furthermore, there is little effect on the passband, and the insertion loss increases by only 0.3 dB, making the proposed filter concept suitable for LE-based realization.

We chose a second-order BPF with a center frequency of 1.2 GHz and a fractional bandwidth of 73% (i.e., the bandwidth of the BPF without the notch present) to realize the proposed concept. Because the BSF sections were directly connected to the BPF resonators, the resulting in-band notch was also second order. Furthermore, the resulting notch has a fractional bandwidth of approximately 7.3%. Although the competition objectives called for minimal loss in the passband from 1.1 to 1.3 GHz, no specifications were given for the bandwidth of the passband or its selectivity. Therefore, to reduce insertion loss and simplify the design, we chose a wide fractional bandwidth of 73% for the passband response.

The coupling routing diagram can be realistically implemented using LEs, as shown in Figure 2(b). The resonators can be simply modeled as parallel-type LC resonators (L_R and C_R) and the couplings between resonators as impedance/admittance inverters, which are realized by their low-pass π-type equivalent (L_P and C_P) [12]–[14], [16]. Other types of impedance inverters (e.g., low-pass T type or high-pass π type) could also have been used; however, because of the low Q_U of the LE-based inductors, we selected the low-pass π-type equivalent, because it is based on only one inductor per coupling element. To decrease the number of elements and further miniaturize the filter, the parallel-type resonators in the bandstop sections were transformed through their connecting impedance inverters and equivalently realized as series-type LC resonators (L_S and C_S), as shown in Figure 2(b) [14]. We incorporated frequency variability into these bandstop sections by using tunable varactors (D_S) for C_S.

We designed the RF filter as follows. The normalized coupling coefficients in (1) were first denormalized using

$$M'_{(i,j)} = \frac{M_{(i,j)}}{Z_0}, \tag{2}$$

where Z_0 is the system reference impedance (50 Ω in this case) and $M'_{(i,j)}$ is the required denormalized

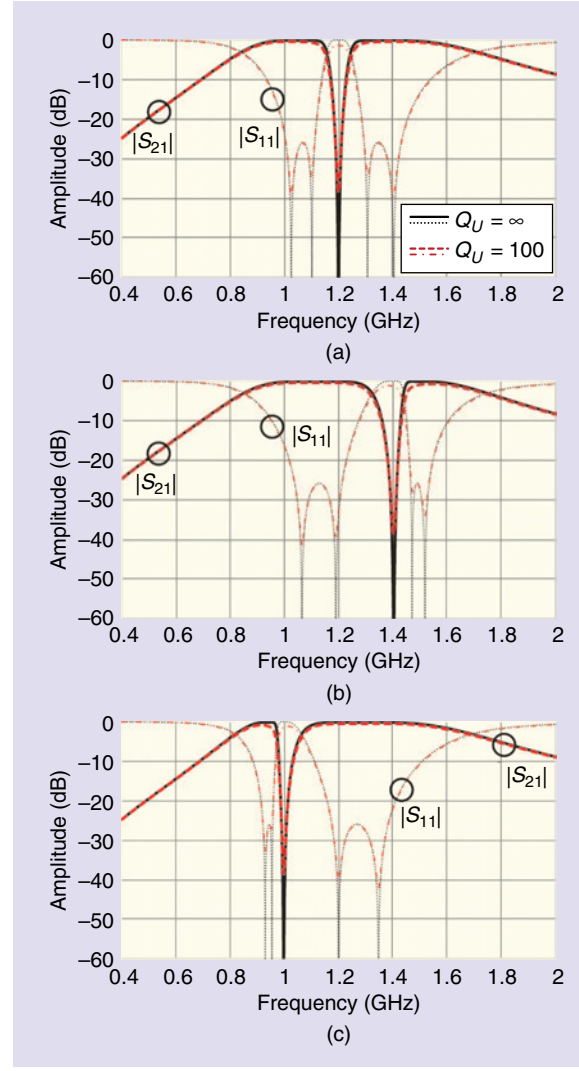

Figure 3. *The theoretically synthesized power transmission ($|S_{21}|$) and reflection ($|S_{11}|$) responses of the coupling routing diagram in Figure 2(a) as the spectral location of the stopband, f_{BS}, is varied. (a) $f_{BS} = 1.2$ GHz, $M_{33} = M_{55} = 0$. (b) $f_{BS} = 1.4$ GHz, $M_{33} = M_{55} = -0.43$. (c) $f_{BS} = 1.0$ GHz, $M_{33} = M_{55} = 0.51$. For the lossy resonator cases, $-j0.014$ was added to M_{22}, M_{33}, M_{44}, and M_{55} to account for a Q_U of 100.*

coupling coefficient. The effective characteristic impedances of the internode couplings (i.e., realized as impedance inverters with impedance $Z_{i,j}$) were then calculated using (3):

$$Z_{(i,j)} = \frac{1}{M'_{(i,j)}}. \tag{3}$$

The LE values of the low-pass π-type networks can be found from the impedances, $Z_{i,j}$, and the frequency of operation, ω_0 [16]:

$$C_P = \frac{1}{\omega_0 * Z_{i,j}}$$
$$L_P = \frac{Z_{i,j}}{\omega_0}. \tag{4}$$

Next, the component values for the parallel-type resonators in the bandpass section, C_R and L_R, were determined based on

$$C_R = \frac{1}{\omega_0 * FBW * Z_0}$$
$$L_R = \frac{1}{\omega_0^2 * C_R}, \tag{5}$$

where FBW is the fractional bandwidth of the overall passband (0.73 in this case).

When unrealistic or impractical values were obtained using this method, the component values of a resonator could be scaled if the impedances of the impedance inverters that are connected to it were also scaled using

$$k = \frac{C'_R}{C_R}$$
$$M''_{i,j} = M'_{i,j} * \sqrt{k}, \tag{6}$$

where C'_R is the desired capacitance of the resonator, k is the ratio of C'_R and C_R, and $M''_{i,j}$ is the newly scaled coupling coefficient. Equations (3)–(5) were then reused with C'_R and $M''_{i,j}$ to find the newly scaled component values. The component values of the series-type resonators in the BSF sections were found using

$$C_S = L_R * M'^2_{i,j}$$
$$L_S = \frac{C_R}{M'^2_{i,j}}, \tag{7}$$

where $M'_{i,j}$ is the denormalized coupling coefficient of the section's impedance inverter.

As is common for all LE circuits, the values of the elements were altered in the physical implementation to account for parasitics. The complete circuit schematic of the proposed filter is shown in Figure 2(c). Although we implemented the BPF section directly, as previously mentioned, we had to make minor changes to the bandstop sections to account for biasing the varactor diodes, D_S. The dc-blocking capacitors, C_{DC}; RF chokes, L_{DC}; and dc voltage supplies were added for the biasing network. The series-resonance capacitance, C_S, is realized as the combination of the varactor, D_S, and the dc-blocking capacitor, C_{DC}.

The manufactured prototype is shown in Figure 4. It was manufactured using an LPKF S103 milling machine on a Rogers RO4003C substrate with dielectric permittivity $\varepsilon_r = 3.38$, dielectric thickness $H = 1.52$ mm, and dielectric loss tangent $\tan\delta_D = 0.0021$ [17]. The design and electromagnetic (EM) simulations of the filter were completed using the Advanced Design System software package from Keysight. The components used are listed in Table 1. All inductors and capacitors used are from Coilcraft [18] and AVX's MLO series [19], respectively; varactor diodes from Skyworks' SMV123x series [20] were used for tuning. The LE integration scheme resulted in a compact filter size of 20×9.4 mm^2 (i.e., 1.88 cm^2).

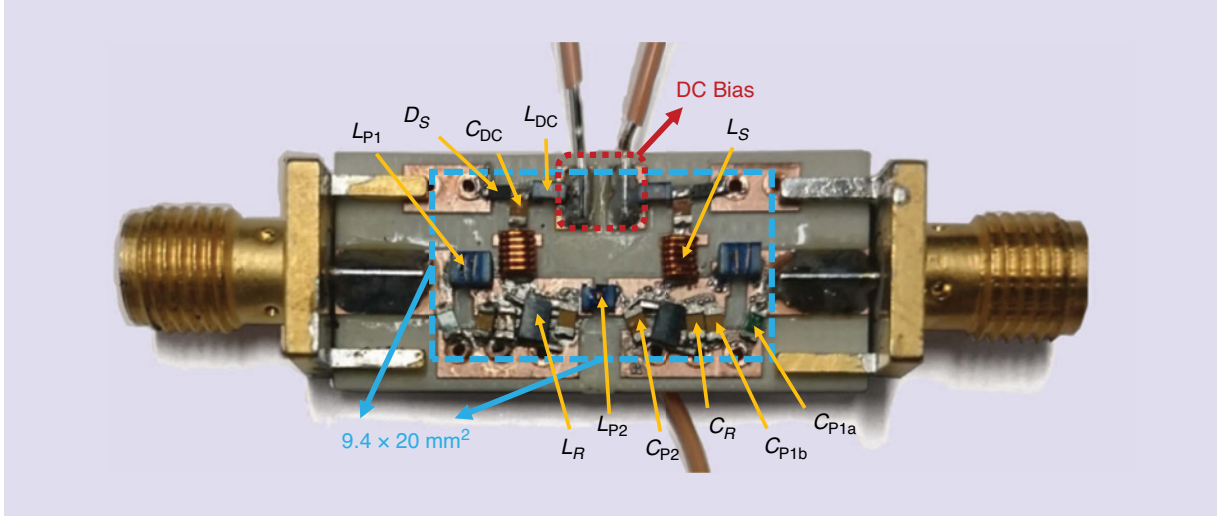

Figure 4. *The manufactured filter.*

TABLE 1. The surface-mounted components labeled in Figures 2(c) and 4.

Component	Value	Part Number
C_{P1a}	1.7 pF	ML03V11R7BAT2A
C_{P1b}	3.3 pF	ML03V13R3BAT2A
C_R	0.8 pF	ML03V10R8AAT2A
C_{P2}	3.3 pF	ML03V13R3BAT2A
C_{DC}	3 pF	ML03V13R0BAT2A
L_{P1}	4.7 nH	0805HT-4N7
L_{P2}	2.6 nH	0604HQ-2N6
L_S	15.7 nH	0806SQ-16N
L_R	5.4 nH	0906-5
L_{DC}	150 nH	0603HP-R15
D_S	0.466–2.35 pF	SMV1231

Measured and Simulated Responses of the Proposed BPF with In-Band Interference Suppression

The RF-measured and EM-simulated frequency responses of the manufactured prototype are illustrated in Figures 5 and 6. Figure 5 shows the measured and simulated responses for the three desired interference suppression scenarios, and Figure 6 displays a measured response over a wide frequency range. The measurements were performed using a Keysight 5224A performance network analyzer; the varactor diodes were reverse-biased using a dc power supply with voltage range of 0–15 V.

As illustrated in Figure 5, the measured and simulated responses show good agreement for all states. The bandwidth of the passband is the main difference between the two sets of responses and can be attributed to the LE-component tolerances and the unaccounted coupling between inductors in the EM simulation. Because the bandwidth was designed to be relatively wide, these discrepancies do not affect the desired performance of the filter.

Table 2 summarizes the measured performance metrics for each interference scenario. In particular, at the interfering frequencies, the notch provides a rejection ranging from 47.9 to 66.3 dB, and the minimum passband insertion loss is below 0.73 dB for all measured states. The filter performance for the different interference suppression scenarios is summarized as follows.

- In the 1.2-GHz interfering signal scenario, the insertion loss in the passbands of interest (1.1–1.15 GHz and 1.25–1.3 GHz) was between 1.76 to 10.33 dB, and the notch provided a high rejection of 21.1–47.9 dB in the desired stopband (1.175–1.225 GHz).

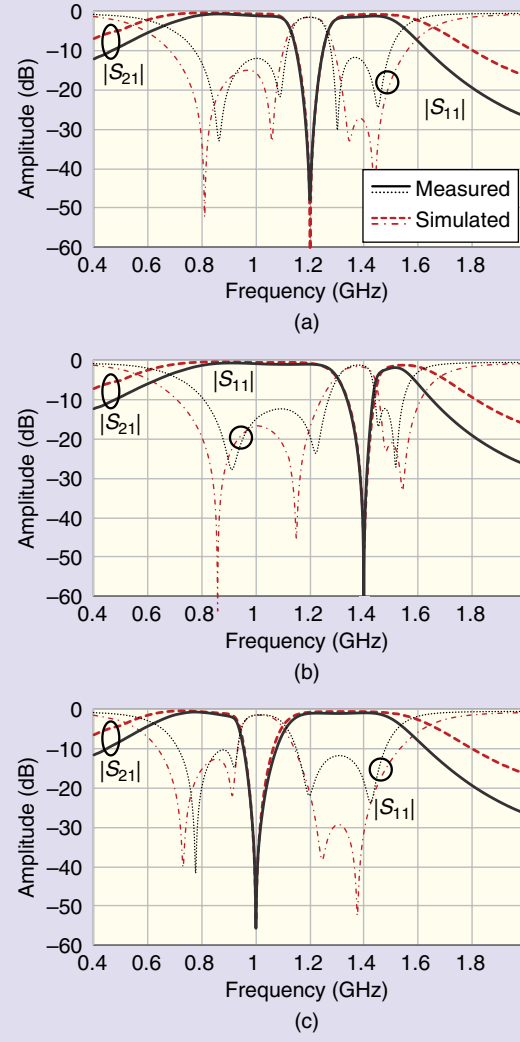

Figure 5. *The EM simulated and RF-measured power transmission ($|S_{21}|$) and reflection ($|S_{11}|$) responses of the manufactured prototype in Figure 4 as the spectral location of the stopband, f_{BS}, is varied: (a) f_{BS} = 1.2 GHz, (b) f_{BS} = 1.4 GHz, and (c) f_{BS} = 1.0 GHz.*

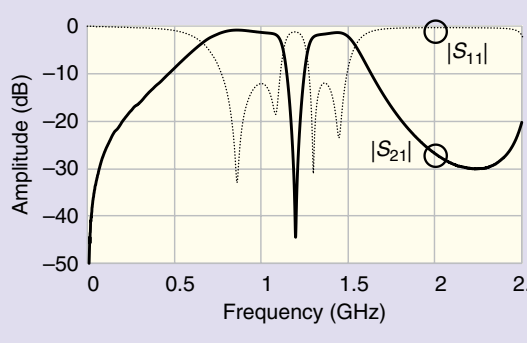

Figure 6. *The measured power transmission ($|S_{21}|$) and reflection ($|S_{11}|$) responses of the manufactured prototype in Figure 4 over a wide frequency range.*

TABLE 2. Summary of the measured performance metrics.

Interference Scenarios (dB)	1.2 GHz	1.4 GHz	1.0 GHz
IL_{min}, passband	0.55	0.51	0.73
IL, 1.1–1.3 GHz	N/A	0.83–4.03	1.01–6.19
IL, 1.1–1.15 GHz	1.76–10.33	0.87–0.88	2.07–6.19
IL, 1.25–1.3 GHz	1.83–9.45	1.26–4.03	1.04–1.10
RL, passband	>11.5	>12	>10
Notch rejection	47.9	66.3	55.8

IL: insertion loss; N/A: not applicable; RL: return loss.

- In the 1.4-GHz and 1.0-GHz interfering signal scenarios, the maximum insertion losses in the passband (1.1–1.3 GHz) were 4.03 and 6.19 dB, respectively, and the notch rejections were 66.3 and 55.8 dB, respectively.

Finally, the filter remained matched throughout the tuning range, with a return loss greater than 10 dB. The performance of the filter could be improved by using distributed elements for the resonators and impedance inverters or by increasing the filter order; however, these would lead to an increase in size, and this design focused on size miniaturization.

Conclusions

This article reported the RF design and practical realization of a compact BPF with an embedded, electronically tunable in-band notch for adaptive interference suppression. We developed the BPF in the context of the IMS 2018 SDC objectives. The proposed filter design is based on a wide-band, second-order BPF with BSF sections incorporated, which results in a tunable in-band notch. The size of the filter is significantly reduced compared with a conventional cascaded-filter approach. To further miniaturize the filter, we used an LE implementation scheme, resulting in a compact filter area of $1.88\ \text{cm}^2$. We incorporated frequency tunability by using varactor diodes from Skyworks in the BSF sections. The presented filter successfully met the competition objectives and received the first-place award in its category. Its RF performance and miniaturized size make it an attractive candidate for reconfigurable radios in the ultrahigh-frequency band that experience dynamic interference.

Acknowledgment

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In Memoriam

John Douglas Adam

On 7 August 2018, John Douglas Adam passed away at the age of 75 after a sudden illness. He was born in Stirling, Scotland, on 21 March 1943 and completed his formal education in Scotland. He earned his B.S and M.S. degrees from the University of Strathclyde and went on to earn a Ph.D. degree in electrical engineering at the University of Glasgow.

Dr. Adam immigrated to the United States in 1977 and joined the Engineering Department at Westinghouse Corporation (now Northrup Grumman Corp.). There he worked on state-of-the-art device developments, including novel signal processing devices based on microwave interactions with epitaxial yttrium-iron-garnet films such as magnetostatic wave (MSW) channelizers, frequency selective limiters (FSLs), and monolithically integrated circulators on semiconductor substrates. Most recently,

Dr. Adam was a science architect in the Advanced Concepts and Technology Division of Northrop Grumman Electronic Systems. His management responsibilities encompassed research and development of miniature filters, microelectromechanical system (MEMS) devices, miniature time standards, ceramic packaging, and crystal growth.

He was a coinventor of the stripline FSL and principal developer of MSW FSLs. He was involved in the development of microwave acoustic and magnetic devices for defense applications, including a switchable chip-scale channelizer for digital beamforming radar, a chip-scale spectrum analyzer, and a 6–24-GHz FSL. As a result of this work, he was awarded 20 patents and authored 70 publications.

Dr. Adam was also active in the IEEE Microwave Theory and Techniques Society (MTT-S). He served as chair of the Technical Coordinating Committee on Ferrites and Ferroelectrics (MTT-13) and was a member of the IEEE MTT-S International Microwave Symposium (IMS) Technical Program Review Committee 2000–2007. He was vice-chair of IMS2011 in Baltimore, Maryland, United States.

Aside from passion for his work, he led an active life, displayed a quiet sense of humor, and had the uncanny ability to fix anything. He was an avid gardener, rower, cook, and runner. He treasured time with his wife and best friend of 49 years, Elspeth, and their sons, Neil and Mark.

Dr. Adam was an IEEE Fellow.

Compiled by Jerry Hausner (jhausner@aol.com), MTT-S Memorials Committee chair.

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Pete Rodrigue

Dr. George Pierre "Pete" Rodrigue (born 19 June 1931) died 9 September 2018 at the age of 87 after a long illness. He spent 28 years of his career teaching electrical engineering at the Georgia Institute of Technology (Georgia Tech), Atlanta, until his retirement in 1996.

Dr. Rodrigue grew up along Louisiana's Bayou Lafourche, in Napoleonville and Paincourtville, and graduated from Napoleonville High School in 1948. He earned his bachelor's and master's degrees in physics from Louisiana State University and a Ph.D. degree in applied physics from Harvard University, Cambridge, Massachusetts.

Dr. Rodrigue worked as a research scientist for Sperry Microwave Electronics Company in Clearwater, Florida, in the late 1950s and 1960s. He and his colleagues won multiple patents, pioneering the development of microwave technologies. As his interests turned toward academia, he became a professor of electrical engineering at Georgia Tech in 1968 and a regents' professor in 1977. Former

students considered him a gentleman and a mentor, willing to solve any engineering problem. Several times he was recognized as the department's outstanding teacher, and in 1972 he was named Outstanding Teacher for all of Georgia Tech. In 1995, he was honored with the IEEE Microwave Theory and Techniques Society (MTT-S) Distinguished Educator award. He served the IEEE in many capacities and was president of the MTT-S for 1975–1976.

A nationally recognized expert in microwave technology, he consulted for prominent organizations such as the Los Alamos National Laboratory, Bell Labs, Hughes Aircraft, Lockheed-Georgia, Raytheon, Northrup, and Airtron. His support for the MTT-S included (in addition to his service as Society president) participating in various Chapter activities and serving as the Society newsletter editor, as an Administrative Committee member (1970–1979), as designated symposium chair and Membership Services chair (1974), and as vice-president for long-range planning (1975). He also jumped in to chair IMS1993 in Atlanta upon the passing of Walter Cox.

Dr. Rodrigue was an avid sailor, taking generations of children and grandchildren out on the Gulf of Mexico and Lake Lanier. He once cited three reasons for becoming a professor: "June, July, and August."

His personal interests included the New York Metropolitan Opera, the Atlanta Opera, and the Atlanta Symphony Orchestra. His true passion was his family. He hosted raucous, politically contentious dinners every evening and gigantic family vacations every summer, while putting six children through college. Dr. Rodrigue is survived by his wife of 63 years, Mary Merritt Rodrigue, their six children, and seven grandchildren. In addition, his legacy continues through the thousands of students he taught and mentored.

Compiled by Jerry Hausner (jhausner@aol.com), MTT-S Memorials Committee chair.

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MicroBusiness *(continued from page 11)*

I had experienced decades earlier. Our chief technology officer had a default view that we should publish nothing and even objected to our reviewing articles, arguing that, based on the comments we did (or didn't) make, we would betray secrets concerning what we were working on.

I still believe that, in this case, it would have posed no risk for us to publish technical details of what we were working on. The timing would work in our favor. We wouldn't have the time to write an article until after our critical project schedules were met. So, by the time we wrote about our work and what we'd written had been peer reviewed and published, our competitors would have already discovered our innovations in a handset on the market, evaluated it, and understood what we had done.

Technical progress is enhanced by the sharing of ideas, of what works and what doesn't. The tremendous commercial success we now see for our technologies is in large part the result of decades of works published, presented, and shared. When people or groups work in isolation, how many times do the same ideas need to be tested? How many times must the same failures be replicated? Is the dearth of publications from our industries the canary in our gold mine? Is today's success leading to tomorrow's demise?

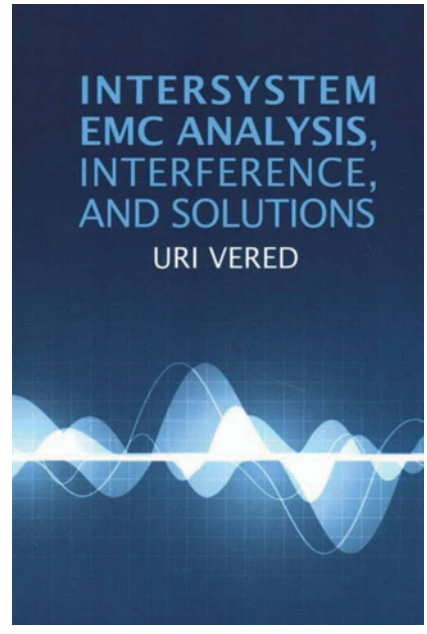
Book/Software Reviews

Learning About Electromagnetic Compatibility

■ **James Chu**

Uri Vered is currently a freelance consultant conducting electromagnetic compatibility (EMC) analysis and seminars in EMC/RF immunity (RFI), wave propagation, wireless communication, and electronic warfare (EW). With more than 50 years of experience in EMC/RFI, wave propagation, and wireless communications and having performed dozens of EMC surveys and studies, mainly for the Israeli defense industry and the Israel Defense Force, he summarizes his practical experience and lessons learned in *Intersystem EMC Analysis, Interference, and Solutions.*

Vered's book on EMC analysis, interference, and solutions discusses intermodulation distortion, but it also covers much more than what an engineer might normally analyze during the design stage. This comprehensive resource provides methods and tools for defining EMC requirements and techniques when predictions and calculations are performed to achieve EMC. The book explores interference from the transmitter or the receiver, between many components, between antennas, and between the receiver and transmitter. It also explains how to calculate interference levels at the receiver, interference margin, and interference probability for the antenna, frequency, and pulse. It goes on to cover interference in digital communication. Finally, the author offers solutions for EMC and interference.



Intersystem EMC Analysis, Interference, and Solutions
by Uri Vered
Artech House, 2018
ISBN-13: 978-1-63081-561-5
329 pages, US$179

The text comprises 23 short chapters running five to ten pages each. All mathematical equations are at the college algebra level—very easy to read and understand. Vered provides many practical examples that illustrate how to solve everyday engineering problems. For instance, engineers often cannot find enough data from manufacturers' data sheets or from system specifications; the text gives an example of using a typical value to complete the work without delay in schedule. All of these shortcuts come from Vered's accumulated knowledge and experience, which are worth more than gold.

The topics covered in each chapter are as follows: Chapters 1 and 2, definitions and EMC requirements; Chapter 3, EMC analysis and survey; Chapter 4, interference types; Chapter 5, interference from both transmitter and receiver; Chapter 6, interference from the transmitter; Chapter 7, interference

(continued on page 118)

James Chu (jameschu@bellsouth.net) is with RF Engineering Consultants, Georgia.

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Around the Globe

2018 MTT-S Chapter Chair Meeting in Poznan

■ **Jan Macháč, Daniel Pasquet, and Wojciech Krzysztofik**

The IEEE Microwave Theory and Techniques Society (MTT-S) organized a Chapter chair meeting on 15 May 2018 in Poznan, a beautiful historical city in Poland, in conjunction with Microwave and Radar Week (MRW), which combined the 22nd International Microwave and Radar Conference (MIKON 2018) and the Baltic International Union of Radio Science Symposium. Representatives of MTT-S Chapters could use a travel grant that covered expenses up to $500 for transportation to and from Poznan and accommodation for two nights. Attendees from the Czech Republic, France, Lithuania, Poland, Russia–Moscow, Russia–St. Petersburg, and Ukraine–West were present, representing their corresponding Chapters.

The aim of this very friendly meeting was to present basic information to Chapter chairs and other Chapter representatives about how to run their Chapter successfully, what they are required to do, and what they can get from the Society and from their Section. The main task of Chapters and their chairs is to represent the Society to their members. That is why the MTT-S takes so much care with Chapter volunteers and organizes these meetings. The meeting also provides a great opportunity for participants to network, meet their colleagues, exchange ideas on good practice, and share their experience.

The meeting was chaired by its organizer, Jan Macháč, Region 8 MTT-S Coordinator (Figure 1). Participants were welcomed by MTT-S President Dominique Schreurs (Figure 2), MRW General Chair Józef Modelski (Figure 3), and Adam Dabrowski, IEEE Poland Section Vice Chair. The main training

Figure 1. *Jan Macháč opens the meeting.*

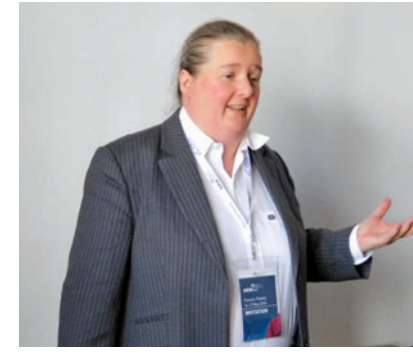

Figure 2. *MTT-S President Dominique Schreurs welcomes the participants.*

Jan Macháč (machac@fel.cvut.cz) is with the Czech Technical University, Prague. Daniel Pasquet (pasquet@ensea.fr) is with Ecole Nationale Superieure de l'Electronique et de ses Applications, Cergy, France. Wojciech Krzysztofik (wojciech.krzysztofik@pwr.edu.pl) is with Wrocław University of Science and Technology, Poland.

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Figure 3. *Microwave and Radar Week Conference General Chair Jozef Modelski welcomes the meeting participants.*

Figure 4. *Daniel Pasquet explains the IEEE structure.*

Figure 5. *Krzystof Kulpa presents the Microwave and Radar Week statistics.*

Figure 6. *Mykhaylo Andriychuk, West Ukraine Chapter chair, presents the Chapter's activities.*

Figure 7. *Adam Dabrowski reports the IEEE Milestone of Prof. Jan Czochralski.*

part of the meeting was conducted by Jan Macháč and MTT-S Member and Geographic Activities Committee Past Chair Daniel Pasquet (Figure 4), who explained the structure of the IEEE and how to manage a Chapter successfully.

Krzystof Kulpa presented the MRW statistics and program (Figure 5), and Wojciech Krzysztofik, IEEE Antennas and Propagation Society (AP)/IEEE Aerospace and Electronics Systems Society (AES)/MTT-S Poland Joint Chapter chair presented his experience heading one of the most successful Chapters in Region 8 and described the activities of the Chapter's very active Chapter members. Mykhaylo Andriychuk, chair of the West Ukraine Chapter, presented the Chapter's history and activities (Figure 6), noting that most of the Chapter's focus is devoted to organizing and supporting particular conferences. Adam Dabrowski talked about the IEEE Milestones program and, in particular, about Prof. Jan Czochralski, inventor of the crystal growth method for semiconductor wafer production (Figure 7).

Figure 8. *Chapter chair meeting attendees. First row from right: Wojciech Krzysztofik, Adam Dabrowski, and Daniel Pasquet.*

The meeting's 16 attendees (Figure 8) discussed the following tasks:

- make Chapter activities interesting to maintain or increase membership
- motivate representatives from industry to participate in Chapter activities
- attract new members and volunteers.

The meeting's organizers thank the MRW organizers for establishing such a warm and pleasant atmosphere. Special thanks go to

- Jacek Misiurewicz, MRW Organizing Chair
- Jan Macháč, MTT-S Region 8 Coordinator, Czech Technical University in Prague, Czech Republic
- Daniel Pasquet, MTT-S MGA Committee Past chair, Region 8 coordinator, Ecole Nationale Supérieure de l' Electronique et de ses Applications, Cergy, France
- Wojciech Krzysztofik, IEEE AP/AES/MTT Poland Joint Chapter chair, Wroclaw University of Technology, Poland.

New Products

■ **Ken Mays, Editor**

Products listed in *IEEE Microwave Magazine* are restricted to hardware, software, test equipment, services, applications, or publications for use in the science and practice of RF/microwave or wireless engineering. Product information is provided as a reader service and does not constitute endorsement by the IEEE or the Microwave Theory and Techniques Society. Absolute accuracy of listings cannot be guaranteed. Contact information is provided for each product so that interested readers may make inquiries directly.

Please submit "New Products" column information to microwave.newproducts@ieee.org.

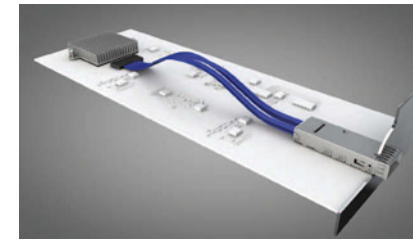
Welcome to a further installment of the "New Products" column in *IEEE Microwave Magazine*. In this issue, we present six new items that may be of interest to the RF/microwave and wireless communities.

Samtec Releases Flyover QSFP28 Cable System

Samtec, a privately held global manufacturer of electronic interconnect solutions, announces the Flyover QSFP28 (FQSFP28) cable system. This new system can support 28-G non–return-to-zero (NRZ)/56-G pulse amplitude modulation (PAM)-4 data rates per each of four channels and provides system design flexibility.

Samtec's FQSFP28 cable system allows sideband signaling via press-fit contacts to improve airflow, reduce loss, and mitigate skew. This system can provide aggregate data rates of 100-Gb/s NRZ/200-Gb/s PAM-4, and it is compatible with all multisource agreement (MSA) quad small-form-factor pluggables. A variety of heat-sink options are available that allow heat dissipation of approximately 3.5 W per cable.

The Samtec FQSFP28 cable system consists of the FQSFP assembly, cage, heat sink, and light pipe. The QSFP offers multiple end-2 options and uses 30- and 34-AWG, 100-Ω eye-speed ultralow-skew Twinax cable. Samtec also offers an FQSFP SI characterization kit for evaluation and development.



"Using the FQSFP series allows for a much longer electrical trace and convenient selection for the endpoint of the SerDes termination," explains Aaron Ram, applications engineer at Samtec, Inc. "The process of routing through the FQFSP series allows designers to locate the QSFP interface much further from the ASIC or processor than traditional printed circuit board routing would allow. This also removes the need for expensive retimers or power-hungry drivers and receivers."

For more information, visit the Flyover QSFP28 cable system web page or download the *Flyover QSFP Application Design Guide*. Immediate technical support is available via e-mail at HDR@Samtec.com.

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Pasternack Releases New Solderless Vertical Launch Connectors with Maximum Operating Frequency up to 50 GHz

Pasternack, a leading provider of RF, microwave, and millimeter-wave products, has introduced a new line of solderless vertical launch connectors that are ideal for high-speed networking, high-speed computing, and telecommunications applications.

Pasternack's new series of vertical launch connectors consists of 12 models that provide a voltage standing-wave ratio (VSWR) as low as 1.3:1 and a maximum operating frequency of up to 50 GHz, depending on the model. These launches contain a reusable clamp attachment and can be used for microstrip or stripline. They are offered in male and female versions, covering 2.4-mm, 2.92-mm, and subminiature-A interfaces, and all models provide solderless installation. These removable vertical launches feature a stainless-steel outer conductor, gold-plated beryllium copper center contact, and polyetherimide insulators. They are ideal for high-speed backplanes, signal-integrity measurements, semiconductor verification boards, multichannel tests, and serializer/deserializer applications.

"The VSWR of these new vertical-launch PCB connectors minimizes the performance tradeoff compared with end launches. This allows our customers to take advantage of additional PCB real estate and allows for easier access for their test cables," says Dan Birch, product manager.

Pasternack's new solderless vertical-launch connectors are in stock and ready for immediate shipment with no minimum order quantity. For detailed information on these products, visit https://www.pasternack.com/pages/rf-microwave-and-millimeter-wave-products/vertical-launch-solderless-connectors.html.

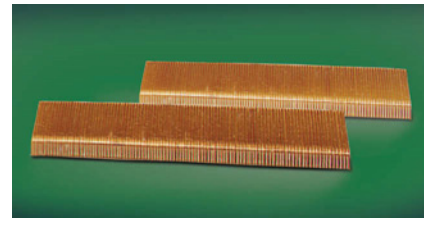
For inquiries, Pasternack can be contacted at +1 949 261 1920.

Low-Resistance Electronic Connector from Fujipoly

Fujipoly Zebra Gold 8000 A elastomeric connectors transfer both data and power between parallel components and circuit boards with a low electrical resistance of lower than 25 mΩ.

This interconnect component is constructed from a low-durometer silicone core wrapped with 100 parallel rows of flat, gold-plated copper wires per inch. This precise construction allows the connector to accommodate PCBs with pad-center spacing down to 0.25 mm. Additionally, each 0.050 × 0.127–mm gold-plated element can deliver a current-carrying capacity of 500 mA.

Fujipoly's Zebra Gold Series 8000 A is a good choice for many board-to-board electronic packaging applications with tight pad-spacing and board-separation tolerances. This connector can be specified in custom lengths from 0.2 to 6.0 in and heights ranging from 0.1 to 0.5 in. For more information, call +1 732 969 0100 or visit http://www.fujipoly.com.



Custom MMIC Launches New Digital Attenuator Product Line Covering DC 40 GHz

Custom MMIC, a leading developer of performance-driven monolithic microwave integrated circuits (MMICs), has launched a new product line of gallium arsenide digital step attenuators (DSAs).

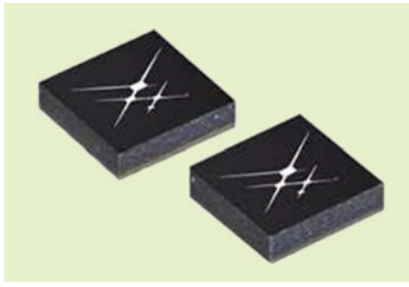
The DSA family is intended to ease the design of high-dynamic-range receivers and instrumentation. These applications often must accomplish gain control of 50 dB or more. Fine-step DSAs (e.g., 0.5-dB least significant bit [LSB]) are often used for these applications. However, when a large attenuation change is needed, it is more efficient to use a lower-bit-count, coarse-step DSA MMIC (e.g., 2-, 4-, or even 8-dB LSB), because this offers lower insertion loss and fewer control lines for easier design implementation.

The eight new products are now available covering up to 40 GHz, with 0.5-, 2-, and 4-dB step-size options. Die- and quad-flat, no-lead packaged versions are available. The CMD281, CMD282, CMD281C3, and CMD282C3 represent initial offerings for coarse-control 2-b DSAs with 2- and 4-dB step control. The CMD279, CMD280, CMD279C3, and CMD280C3 are more traditional 0.5-dB step control devices with a 15.5-dB range (5 b). All devices are single control line per bit.

Visit https://www.custommmic.com/digital-attenuators/for more information and to download full data sheets and S-parameter data.

Skyworks Unveils GNSS LNA Front-End Modules for IoT Applications

Skyworks is pleased to introduce its latest Global Navigation Satellite System (GNSS) low-noise amplifier (LNA) front-end modules, the SKY65933-11 and SKY65943-11. These turnkey GNSS connectivity solutions feature Skyworks' proprietary temperature-compensated



surface acoustic wave filters; are designed specifically for Internet of Things (IoT) applications including smartwatches, action cameras, drones, asset trackers, and personal navigation devices; and can be easily integrated by wireless module and IoT-device manufacturers.

Both modules come in a compact 2.5-mm × 2.5-mm multichip module (MCM) package with surface-mount technology and offer extremely low leakage current (1 µA max)—a key benefit for battery-powered IoT devices. They also integrate a pre- and postfilter LNA and matching to reduce the PCB area versus a discrete implementation as well as a single dc supply for design flexibility and simplicity.

The SKY65933-11 and SKY65943-11 are multi-GNSS compatible, covering GPS, GLONASS, GALILEO, COMPASS (BeiDou), and QZSS receiver applications in the 1,559–1,606-MHz frequency range.

For more information, watch the product video or visit http://www.skyworksinc.com/Product/3578/SKY65933-11.

Analog Devices's 44-GHz Silicon Switches Offer Industry's Lowest Insertion Loss in a Compact Land-Grid Array Package

Analog Devices, Inc., announces production release of its 44-GHz single-pole, double-throw switches, the ADRF5024 and ADRF5025, in advanced silicon-on-insulator technology. The two new switches are broadband, with the ADRF5024 yielding a flat frequency response from 100 MHz to 44 GHz and the ADRF5025 from 9 kHz to 44 GHz, with repeatable characteristics better than 1.7-dB insertion loss and 35 dB-channel-to-channel isolation.

Both parts support 27-dBm power handling for through- and hot-switching conditions. The new switches come in a compact, highly reliable 2.25 × 2.25-mm^2 surface mount technology-compatible package, exhibiting electrical performance beyond incumbent solutions, which will benefit RF and microwave design experts by saving bias power, eliminating peripheral components, and achieving higher integration in systems, such as phased arrays, portable instrumentation, high-resolution body scanners, and next-generation millimeter-wave communication infrastructure for emerging 5G and high-constellation satellite networks.

The ADRF5024 and ADRF5025 use inherent reflective architecture and are characterized for an operating temperature range of –40 to 105 °C. All pins in-

corporate robust electrostatic-discharge protection. The devices are nominally powered by ±3.3 V, typically drawing a low supply current of fewer than 120 µA. The devices use standard positive logic control voltages, simplifying the interface design.

The ADRF5024 and ADRF5025 are ideal replacements for p-i-n diode-based counterparts: no external components are necessary for bias generation or matching, and signal pins are internally biased at ground reference to eliminate the need for dc-blocking capacitors.

The ADRF5024 is optimized for fast switching applications with speeds lower than 10 ns and edge rates at 2 ns; the ADRF5025 is optimized for ultra-wide-band applications with good low-frequency characteristics down to 9 kHz. The other characteristics are the same, so parts are drop-in alternatives to each other and can be used interchangeably on the same PCB footprint.

For more information, visit http://www.analog.com.

Book/Software Reviews *(continued from page 113)*

from the receiver; Chapter 8, calculating the received interference level; Chapter 9, interference margin and its meaning; Chapter 10, the interference and reception ranges; Chapter 11, propagation models for EMC; Chapters 12–14, interference between antennas including coupling between antennas, relative angles between antennas, and antenna gain; Chapter 15, near field definition, calculation, and path loss; Chapters 16–19, probability of interference, including antenna, frequency, and pulse; Chapter 20, pulse interference in digital communication; Chapter 21, interference in synchronous hopping devices; chapter 22, EMC solutions; and chapter 23, EMC testing.

This book was written to support engineers who are doing practical, everyday EMC work—they will learn how to anticipate problems and then define EMC solutions. The mathematical equations all have straightforward, direct solutions. This book is the desk reference every circuit design engineer and system engineer must have. It can improve the quality of design 100%.

Conference Calendar

JANUARY 2019

IEEE Radio & Wireless Week 2019 (RWW 2019) (includes PAWR, RWS, SiRF, TWiOS, and WiSNet and is colocated with ARFTG)
20–23 January 2019
Location: Orlando, Florida, United States

APRIL 2019

IEEE 19th Wireless and Microwave Technology Conference 2019 (WAMICON 2019)
8–9 April 2019
Location: Cocoa Beach, Florida, United States

International Conference on Microwaves for Intelligent Mobility 2019 (ICMIM 2019)
15–17 April 2019
Location: Detroit, Michigan, United States

MAY 2019

IEEE International Microwave Biomedical Conference (IMBioC 2019)
6–8 May 2019
Location: Nanjing, Jiangsu, China

European Microwave Conference in Central Europe (EuMCE 2019)
13–15 May 2019
Location: Prague, Czech Republic

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Journées Nationales Microondes (JNM 2019)
14–17 May 2019
Location: Caen, France

IEEE International Wireless Symposium 2019 (IWS 2019)
19–22 May 2019
Location: Guangzhou, China

12th Global Symposium on Millimeter-Waves (GSMM 2019)
22–24 May 2019
Location: Sendai, Japan

IEEE International Conference on Numerical Electromagnetic and Multiphysics Modeling and Optimization 2019 (NEMO 2019)
29–31 May 2019
Location: Boston, Massachusetts, United States

JUNE 2019

International Microwave Symposium (IMS 2019; colocated with RFIC2019 and Spring ARFTG 2019)
3–7 June 2019
Location: Boston, Massachusetts, United States

IEEE Wireless Power Transfer Conference 2019 (WPTC 2019)
18–21 June 2019
Location: London, United Kingdom

IEEE PELS Workshop on Emerging Technologies: Wireless Power (WoW 2019)
18–21 June 2019
Location: London, United Kingdom

JULY 2019

Second International Workshop on Mobile Terahertz Systems (IWMTS 2019)
1–3 July 2019
Location: Duisburg, Germany

SEPTEMBER 2019

44th International Conference on Infrared, Millimeter, and Terahertz Waves (IRMMW-THz 2019)
1–6 September 2019
Location: Paris, France

14th European Microwave Integrated Circuits Conference (EuMIC 2019)
29 September–4 October 2019
Location: Paris, France

OCTOBER 2019

49th European Microwave Conference (EuMC 2019)
1–3 October 2019
Location: Paris, France

IEEE International Symposium on Phased Array Systems and Technology 2019 (PAST 2019)
15–18 October 2019
Location: Waltham, Massachusetts, United States

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IEEE Wireless and Microwave Technology Conference

WAMICON 2019
April 8th and 9th 2019
Hilton Cocoa Beach
Cocoa Beach, Florida

Submission Deadline: Friday February 8, 2019

The 20th annual IEEE Wireless and Microwave Technology Conference (WAMICON 2019) will be held in Cocoa Beach, Florida on April 8th and 9th 2019. The conference will address up-to-date multidisciplinary research needs and interdisciplinary aspects of wireless and RF technology. The program includes both oral and poster presentations as well as tutorials and special sessions. Prospective authors are invited to submit original and high-quality work for presentation at WAMICON 2019 and publication in IEEE Xplore. Conference website is www.wamicon.org

TOPICS OF INTEREST INCLUDE

The central theme of WAMICON2019 will be "*Simulation Driven Design of Emerging Wireless, Microwave and mm-Wave Circuits and Systems*". Submissions on all aspects of related technologies, including antennas, passive and active circuits, communication theory, and system concepts, are encouraged.

mm-Wave to THz Technologies

5G Communications, Backhaul, MIMO and Massive MIMO, Beamforming, Vehicle-to-Everything (V2x), SatCom, Human Body Scanners, Radar, Home/Office Application, Electronic Warfare (EW), Tactical Networks/Data Links, Packaging, Integrated Circuits

Internet of Things (IoT)

Smart Homes, Smart Cities, Machine-to-Machine (M2M), Bluetooth Low Energy (BLE), Light Fidelity (Li-Fi), Near-Field Communication (NFC), RFID, Zigbee, Low-Power Wide-Area Network (LPWAN), Active Denial, Cognitive Radios and Software Defined Radios

Power Amplifiers, Other Active Components, and Systems

High-Efficiency PAs, Linearization and Efficiency Enhancement Techniques, Novel PA Architectures, High-Power Devices, Linear/Nonlinear Device Modeling, Reliability/Thermal Considerations, Transceiver Design, Multi-Band and Digital RF Circuits and Systems, System-On-Chip, System-In-Package, Radar RF/MMIC Electronics, Active Filters

Passive Components and Antennas

Filters, Transmission Line Components, MEMS, Advanced Packaging, Antennas and Arrays, Meta-Materials, Frequency Selective Surfaces, Non-Foster Impedance Matching

Microwave Applications

Biomedical Applications, Wireless Sensing, Energy Harvesting, Wireless Power Transfer, Radar, Additive Manufacturing, RF Applications in Space Exploration, Aerospace Applications of RF Circuits and Systems

PAPER SUBMISSION INSTRUCTIONS

Authors are asked to submit papers electronically in .PDF format. In order to be considered for publication by the Technical Program Committee, a submission of 3-4 pages, clearly describing the concept and results must be submitted before the deadline of February 8, 2019. The conference webpage at www.wamicon.org has complete details of submission requirements. Submissions will be evaluated for originality, significance of the work, technical soundness, and interest to a wide audience.

Papers Due:	**Fri., Feb. 8, 2019**
Author Notification:	**Fri., Feb. 22, 2019**
Final Papers Due:	**Fri., Mar. 1, 2019**

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Radio & Wireless Week

26-29 January 2020
San Antonio, TX

http://www.radiowirelessweek.org

Call for Papers

The 2020 Radio & Wireless Week (RWW) will jointly host the 2020 Radio & Wireless Symposium (RWS) and the 20th IEEE Topical Meeting on Silicon Monolithic Integrated Circuits (SiRF2020). Topical meetings held in parallel will provide more focused sessions in the areas of RF Power Amplifiers (PAWR), Wireless Sensors and Sensor Networks (WiSNet), and the Topical Workshop on Internet of Space (TWIOS). Submissions due late July 2019.

RWS

Wireless technologies, emerging applications and systems, medical and environmental sensing, packaging, antennas, novel/ printed materials.

SiRF

CMOS and Si/SiGe BiCMOS technologies for micro- and millimeter-wave applications. From materials to circuits and systems.

PAWR

High power and wide band devices/circuits for mobile, space, and avionic applications. MMICs/Hybrids, modeling, pre-distortion & packaging.

WiSNet

Communications, radar, positioning, imaging, localization & tracking. RFIDs, sensor network topologies, Six-Port & Multi-Port Technology. Body area networks/IoT.

TWIOS

Small/micro Sats & CubeSats; Satellite Constellations, Unmanned Air Systems; Radiation Effects, High Data Rate Links, Geolocation, Earth Observation, SIGHT

Call for Workshops

In addition to the sub-conference topics above, we invite proposals on:

1. RF/Microwave Power Amplifiers
2. Silicon Monolithic Integrated Circuits in RF Systems
3. Wireless Sensors and Sensor Networks
4. Technology for CubeSats and COTS for New Space
5. RF and Microwave Measurement Techniques and Test Beds

Workshop Proposals should focus on a timely topic of high interest to the MTT-S community and encompass a coherent theme that is presented by selected experts in the field. Workshops should be structured and moderated by the organizer so that the audience is actively engaged and, where appropriate, include tutorial or review material to assist the attendees without current knowledge of the subject. We will be able to accommodate up to two full day workshops on Monday and we would like to offer several half-day workshops on Sunday.

Call for Demos

The RWS Demonstration Track provides an interactive forum for hands-on demonstration of your latest wireless experiments and innovations. We invite you to show off your latest innovations live!

Paper submission instructions can be found at http://www.radiowirelessweek.org. Submissions should be formatted according to the template on the RWW website. Authors should indicate their preference for oral or poster presentation. All submissions must be received by late July 2019. All accepted papers will be published in a digest and will be included in the IEEE Xplore® Digital Library. Submissions will be evaluated based on novelty, significance of the work, technical content, interest to the audience, and presentation.

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